Accurate Simulation of EV/HEV Power Electronics Switching Events for HIL Testing

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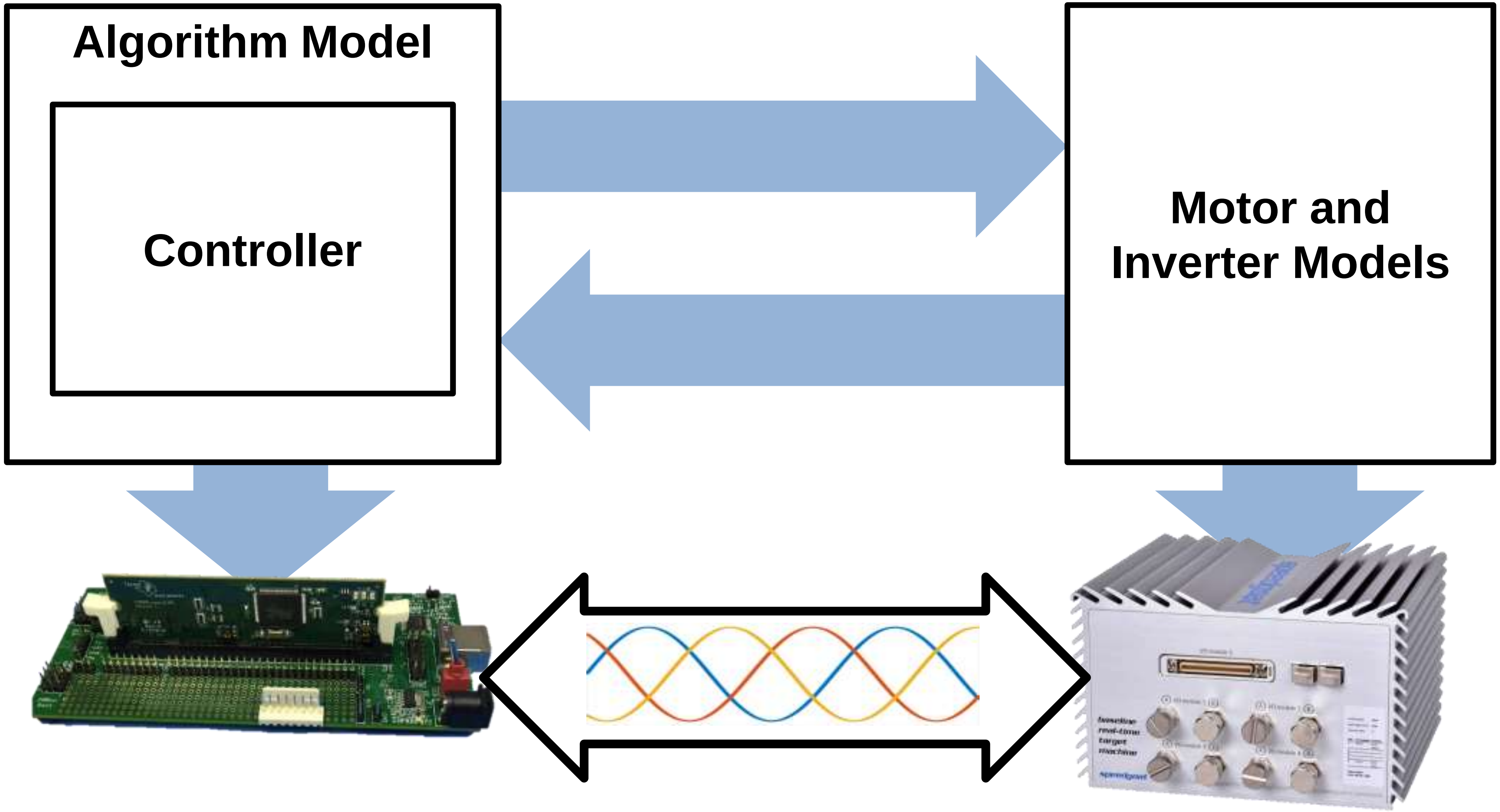
Application Engineer

Overview

1. Hardware-in-the-loop (HIL) overview
2. Review of a system level model of a motor and inverter in Simulink
3. Use of HDL Coder to generate floating-point HDL from the Simulink model to achieve 1 MHz simulation (1 µs time-step)
4. HIL simulation using Simulink Real-Time and Speedgoat target hardware

What is HIL

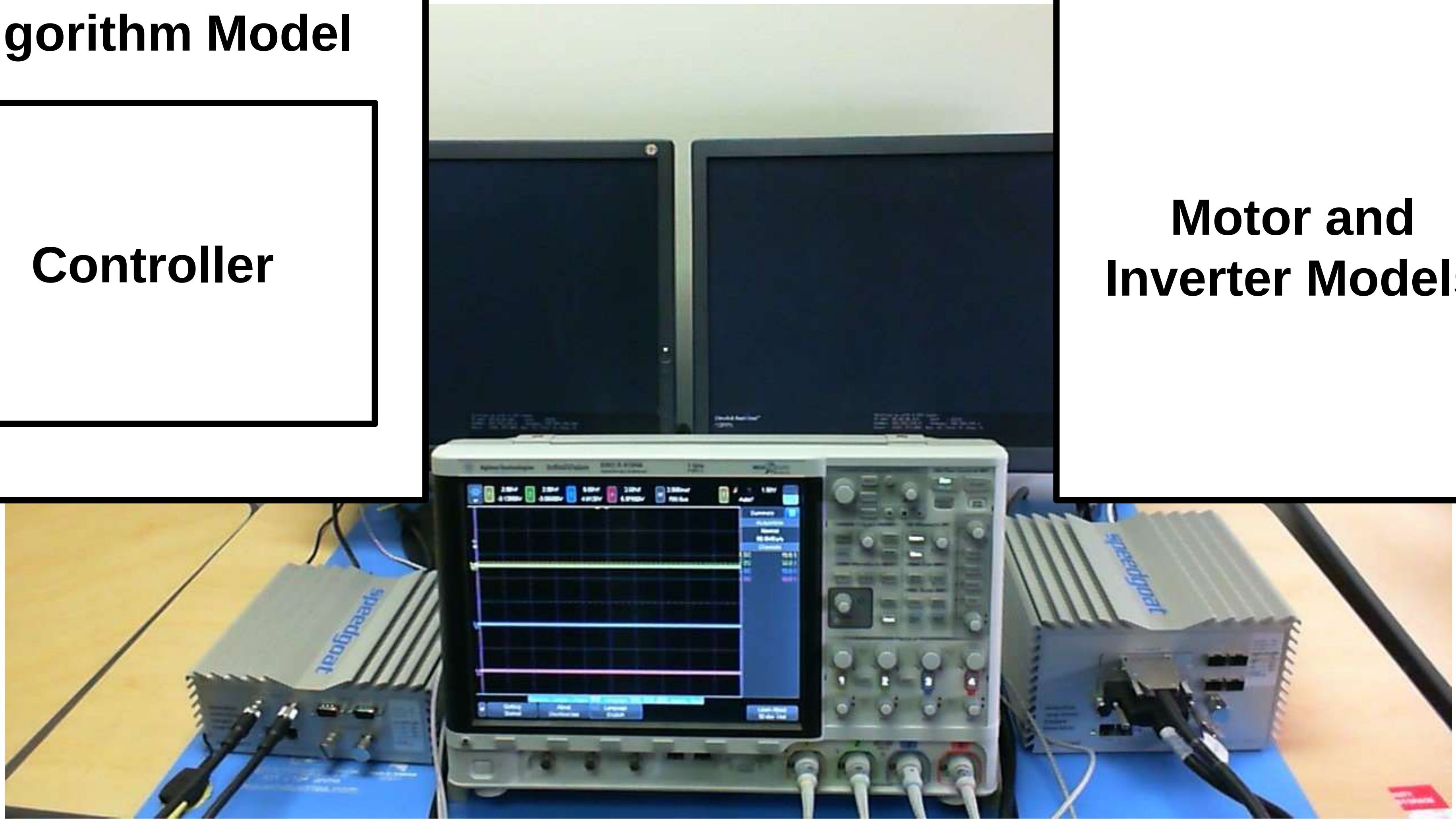


Demo

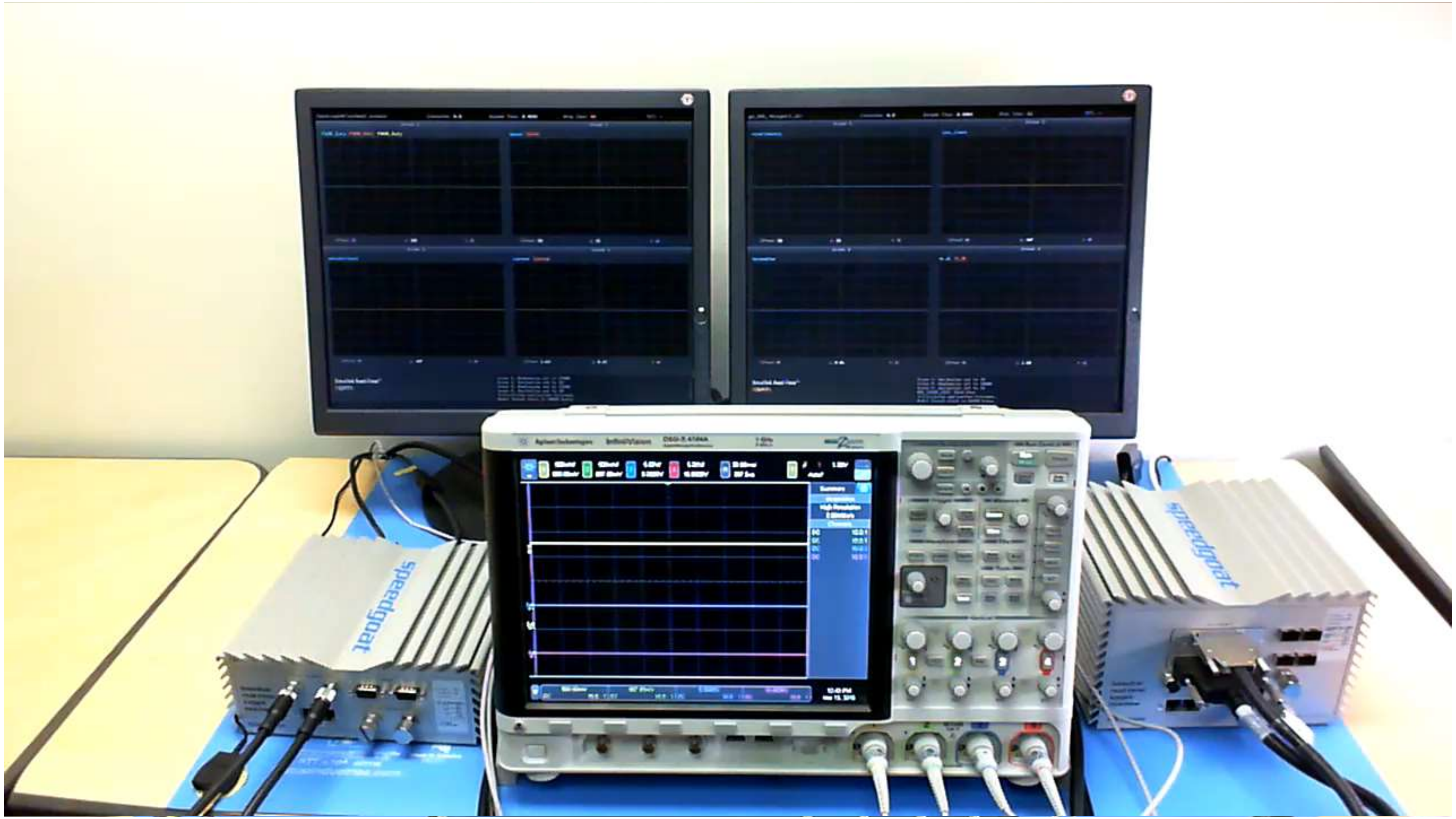
Algorithm Model

Controller

Motor and Inverter Models



Demo



Why HIL?

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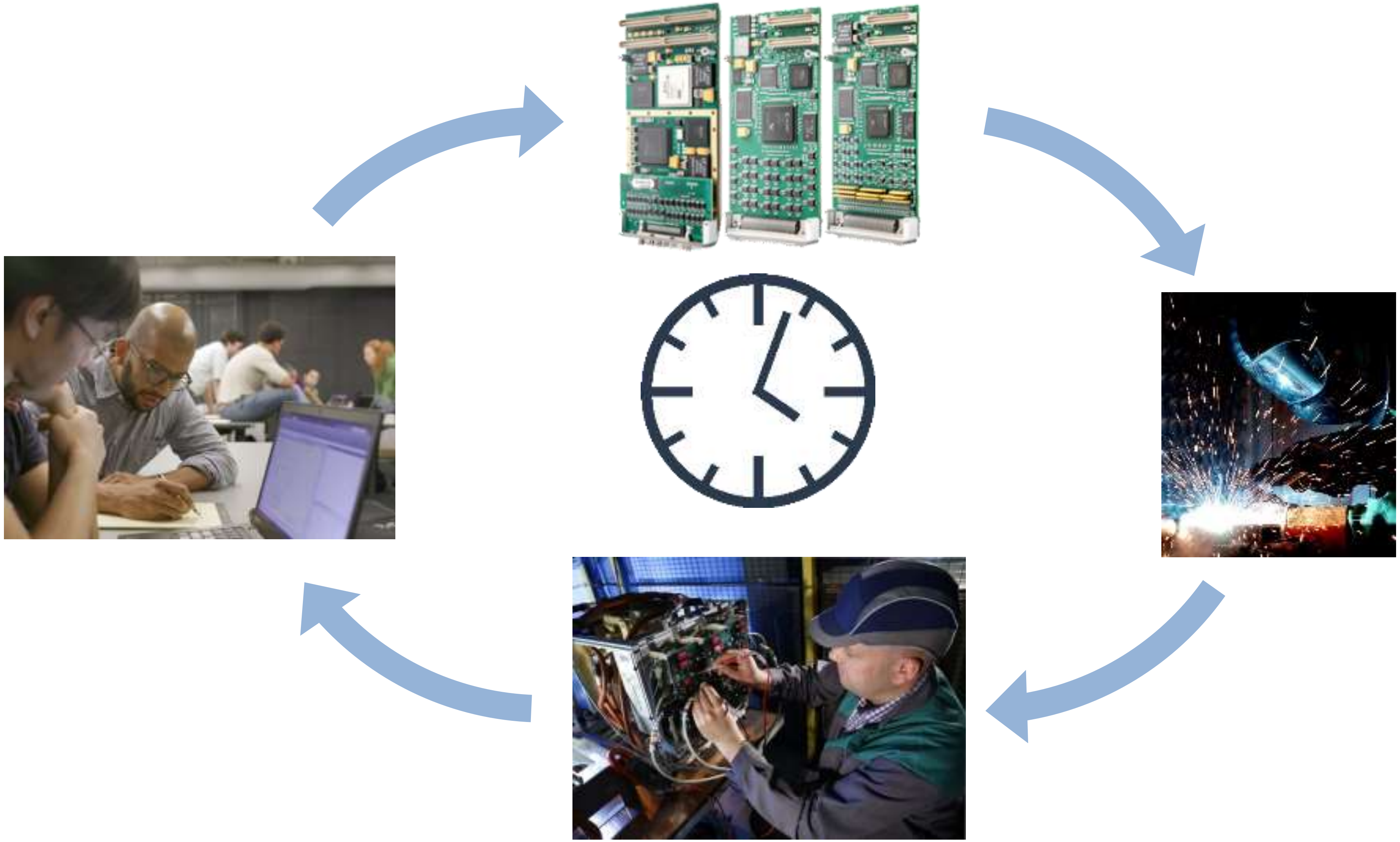
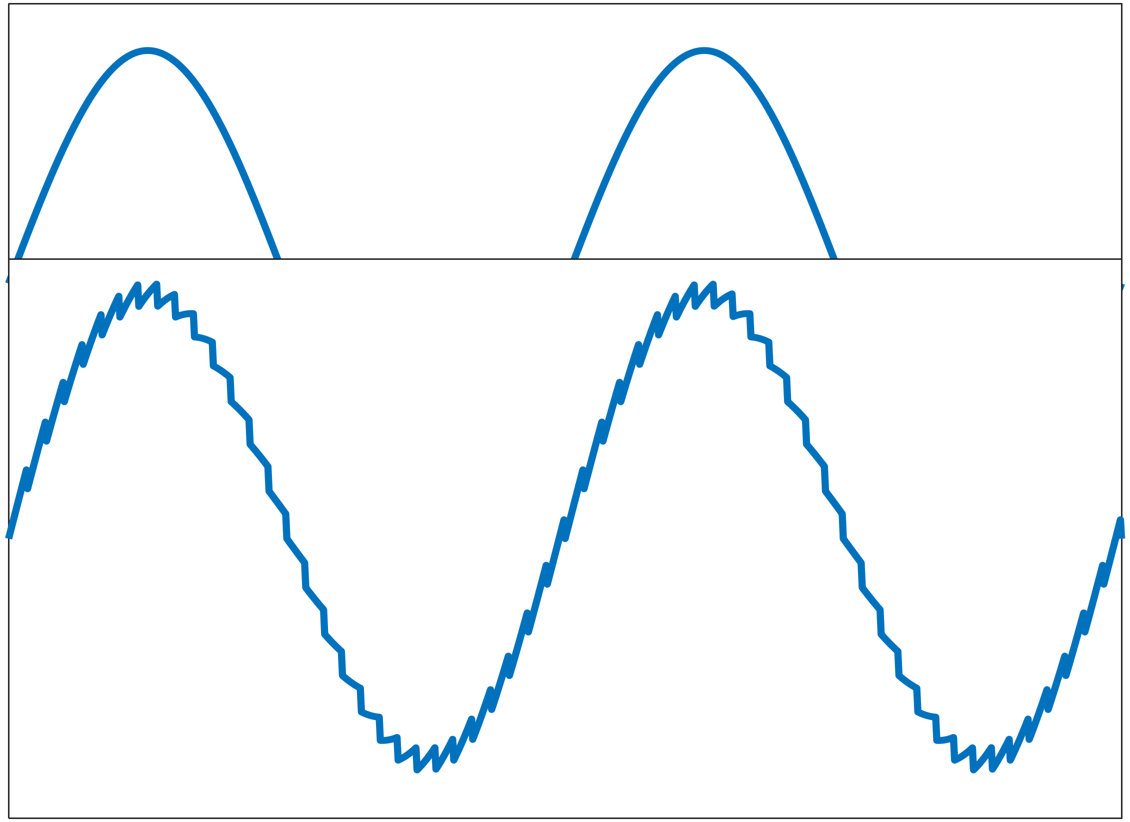


Power Electronics and Motor Control - Switching

2 ways to simulate power electronics

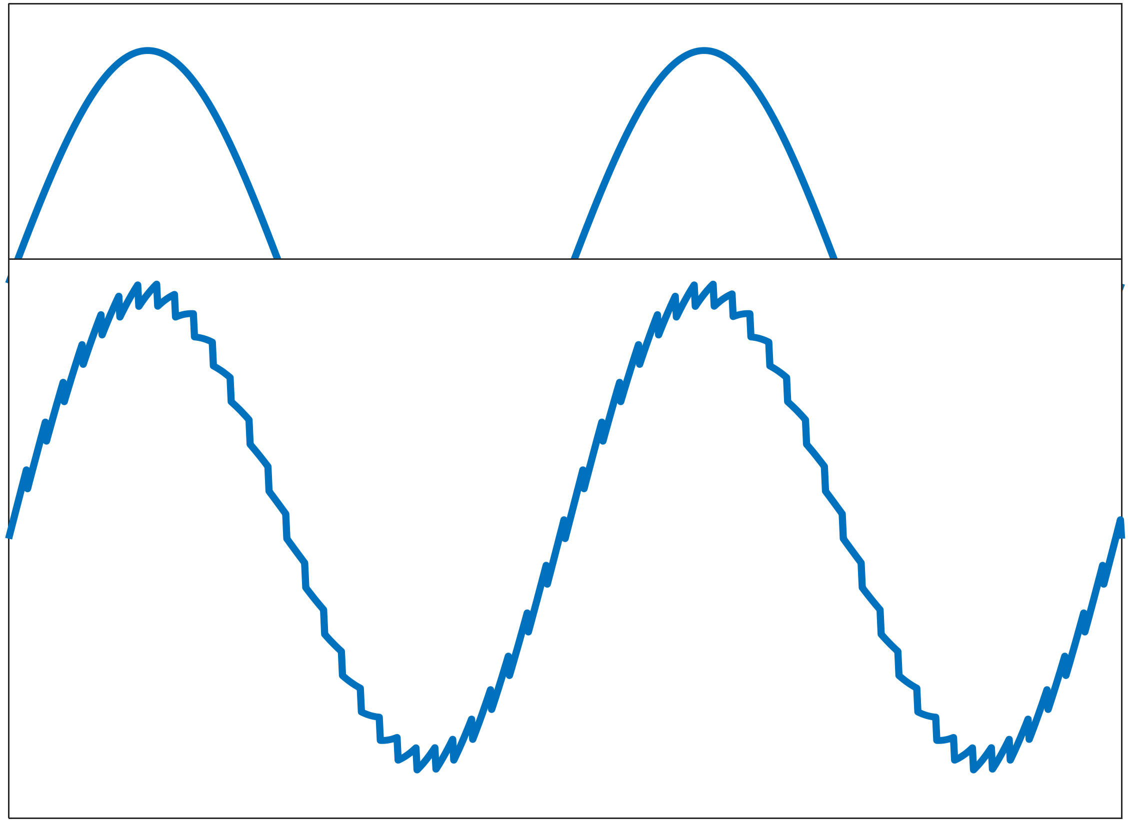
- Average
  - Easy to implement in real time
  - Ignores dynamics of switching devices
  - Good enough for some types of analysis
- Switching
  - Captures switching events
  - Model faults and analyze switching efficiency
  - Requires simulation 100 times faster than switching frequency
  - Motor at 10 kHz requires 1 MHz simulation



CPU vs FPGA Simulations

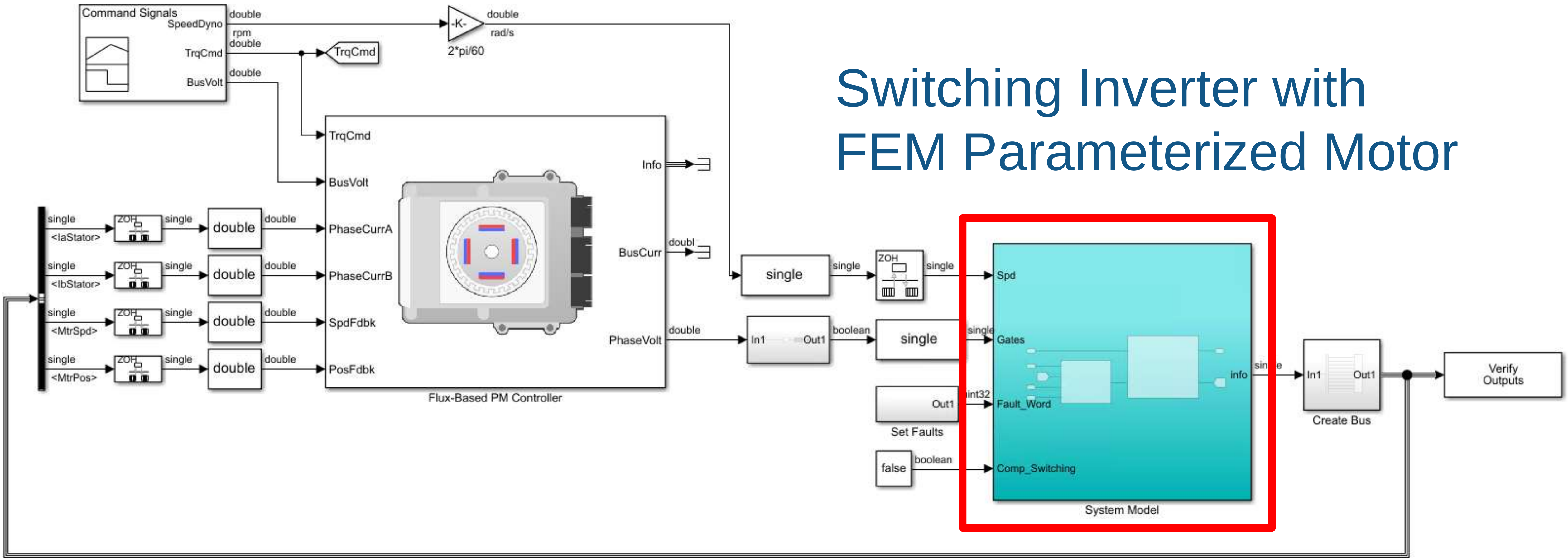
2 ways to simulate power electronics

- CPU
  - Cheaper hardware
  - Can run continuous domain simulation
  - Run any code gen compatible block
  - Good for 10 kHz simulation
  - Use C coder tools to automate
- FPGA
  - Multiple orders of magnitude faster
  - Requires discrete domain simulation
  - Uses sin… floating point values
  - …imulation
  - …e



Review of a System Level Model of a Motor and Inverter in Simulink

Switching Inverter with FEM Parameterized Motor



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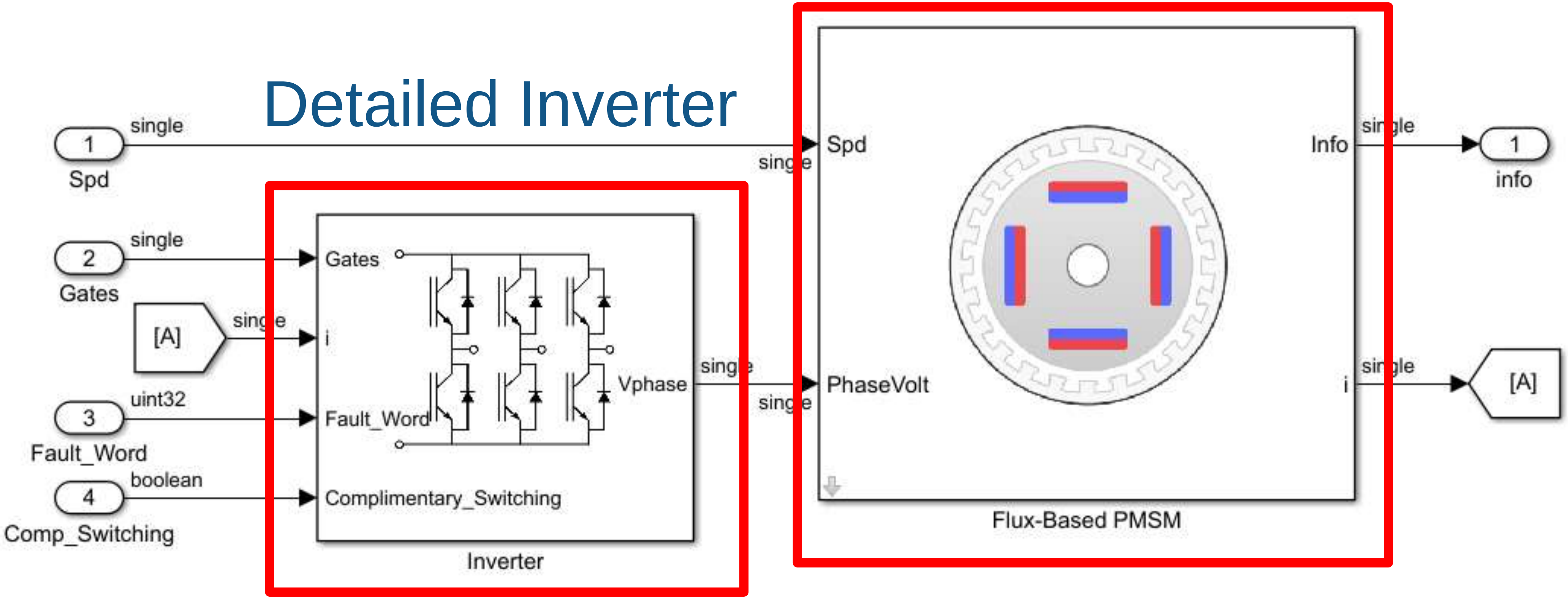
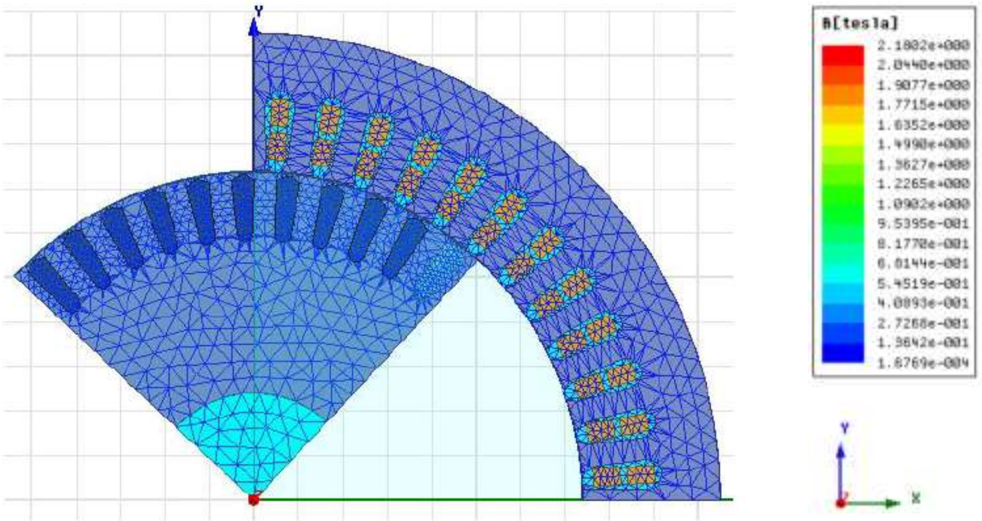
Review of a System Level Model of a Motor and Inverter in Simulink

FEM Based
Motor Model

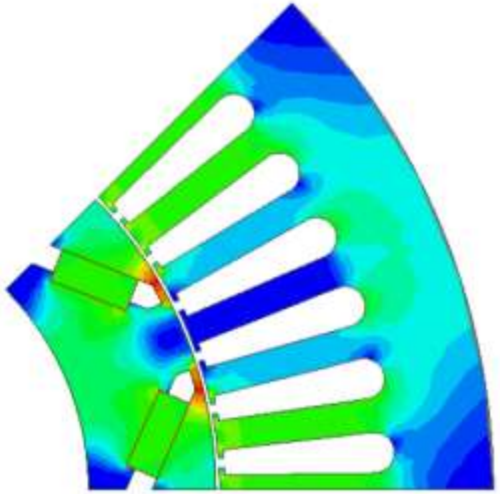
Detailed Inverter



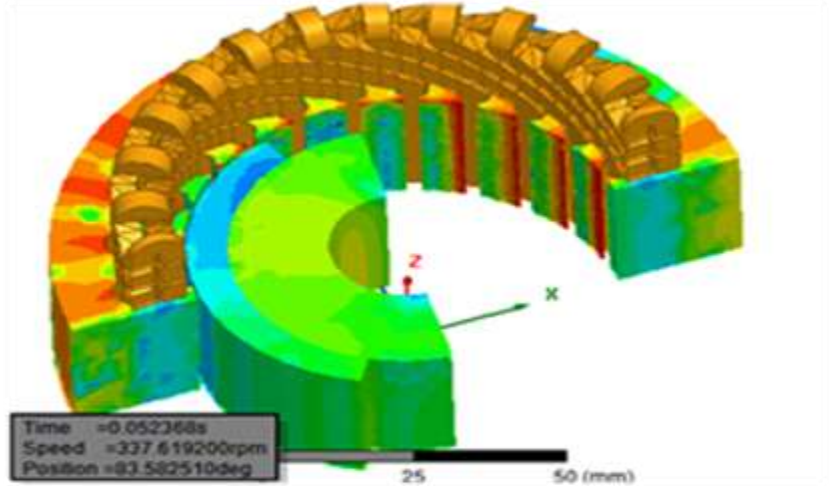
Can Extract Lookup Table from FEM Tool



FEA Meshing for Induction Machine

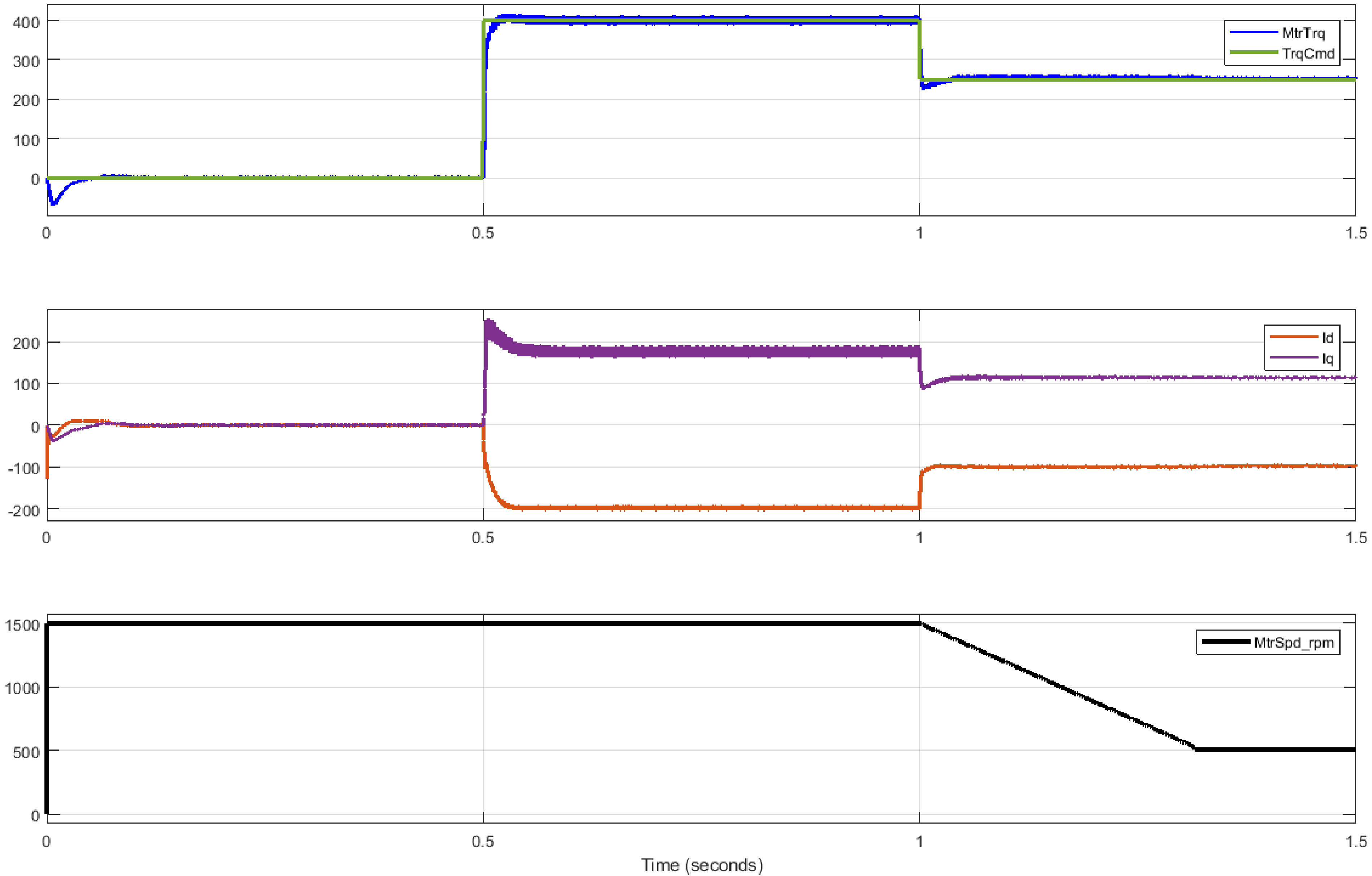


2D FEA PMSM Model



3D FEA PMSM Model

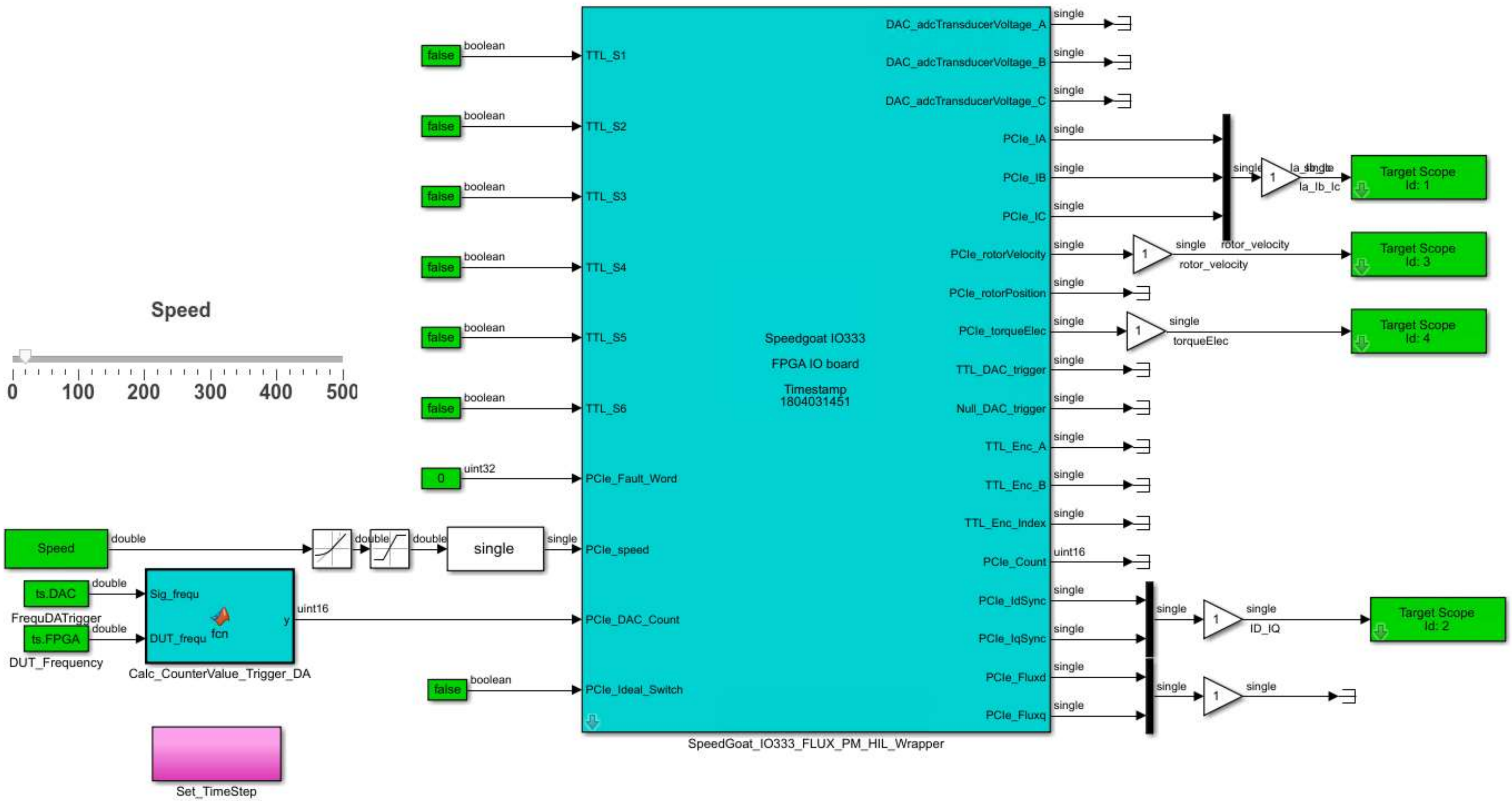
Simulation Results



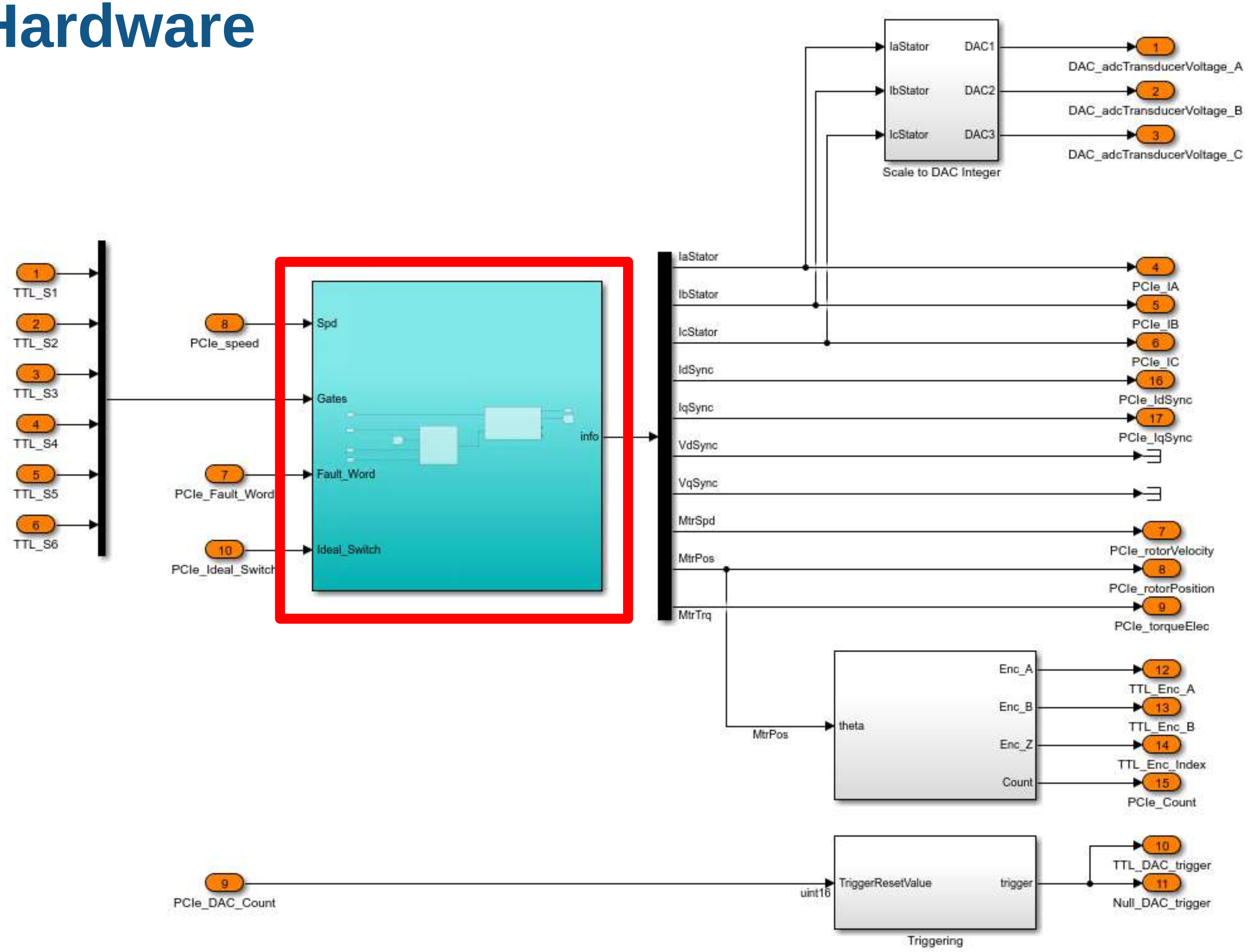
High Level Process for Deploying Model to FPGA

1. Create high level subsystem for defining I/O
2. Convert model to discrete time
3. Convert to single precision
4. Use HDL workflow advisor to setup model settings
5. Deploy model to the Speedgoat real-time machine

HIL Simulation Using Simulink Real-Time and Speedgoat Target Hardware

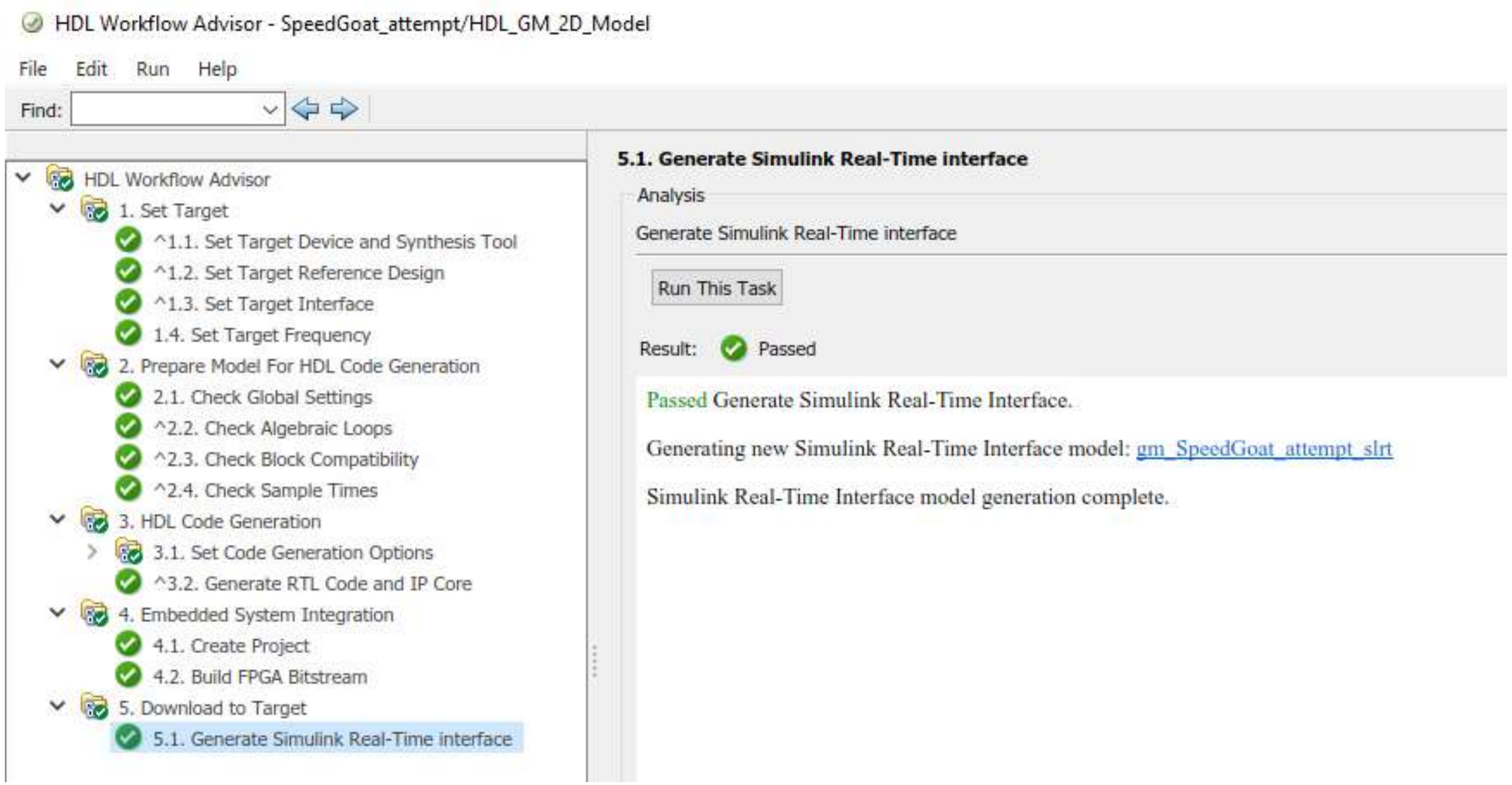


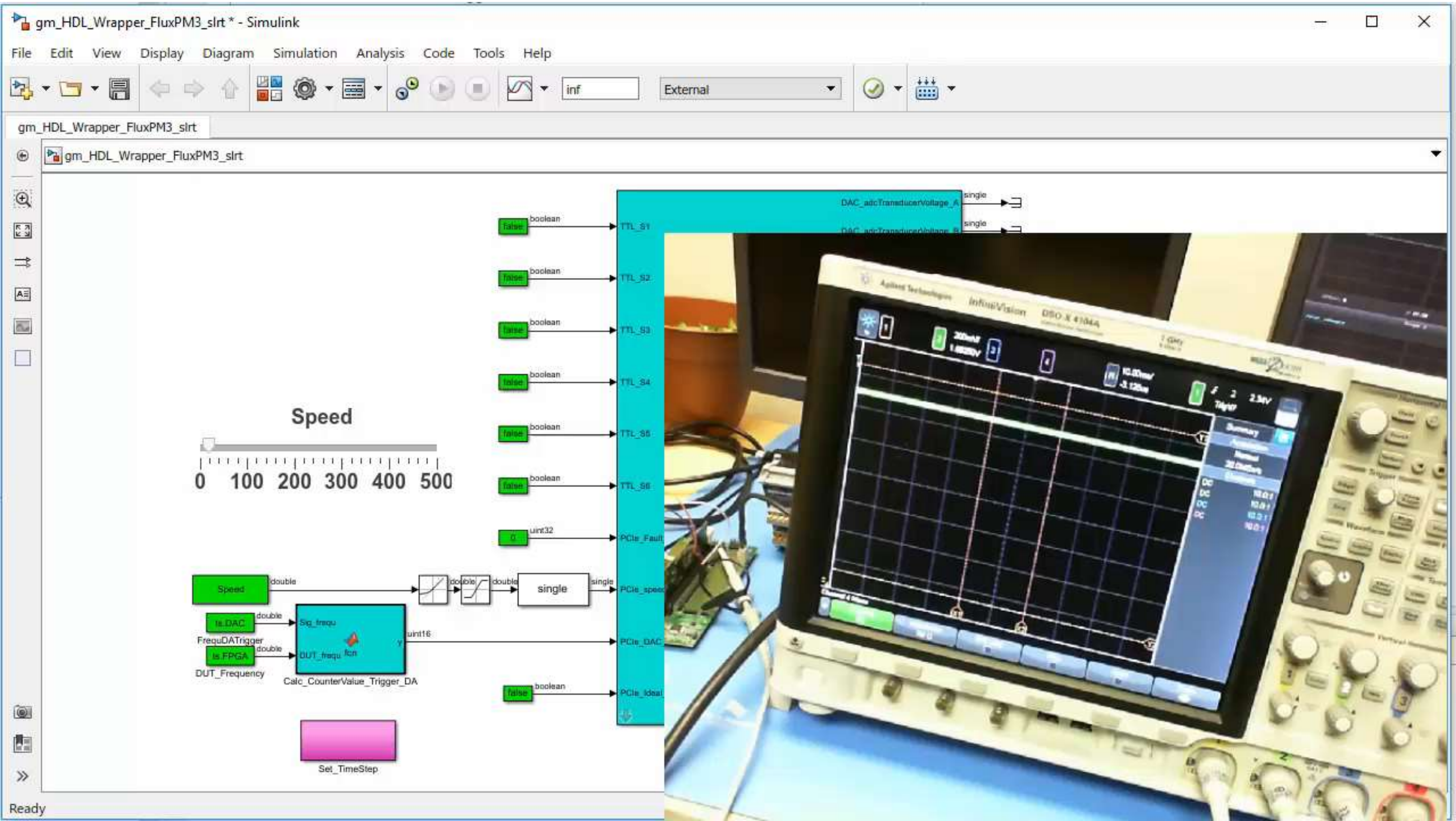
HIL Simulation Using Simulink Real-Time and Speedgoat Target Hardware



Use of HDL Coder to Generate Floating-Point HDL From the Simulink Model to Achieve 1 MHz Time-Steps

Example walkthrough available through webinar:
https://www.mathworks.com/videos/hardware-in-the-loop-hil-testing-for-power-electronics-systems-modeled-in-simulink-1522417541924.html





gm_HDL_Wrapper_FluxPM3_slrt * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
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External
gm_HDL_Wrapper_FluxPM3_slrt
gm_HDL_Wrapper_FluxPM3_slrt
Speed
0 100 200 300 400 500
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boolean
TTL_S1
TTL_S2
TTL_S3
TTL_S4
TTL_S5
TTL_S6
uint32
PCIe_Fault
DAC_adcTransducerVoltage_A
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Speed
double
single
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FrequDATrigger
Is.FPGA
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Sig_frequ
DUT_frequ
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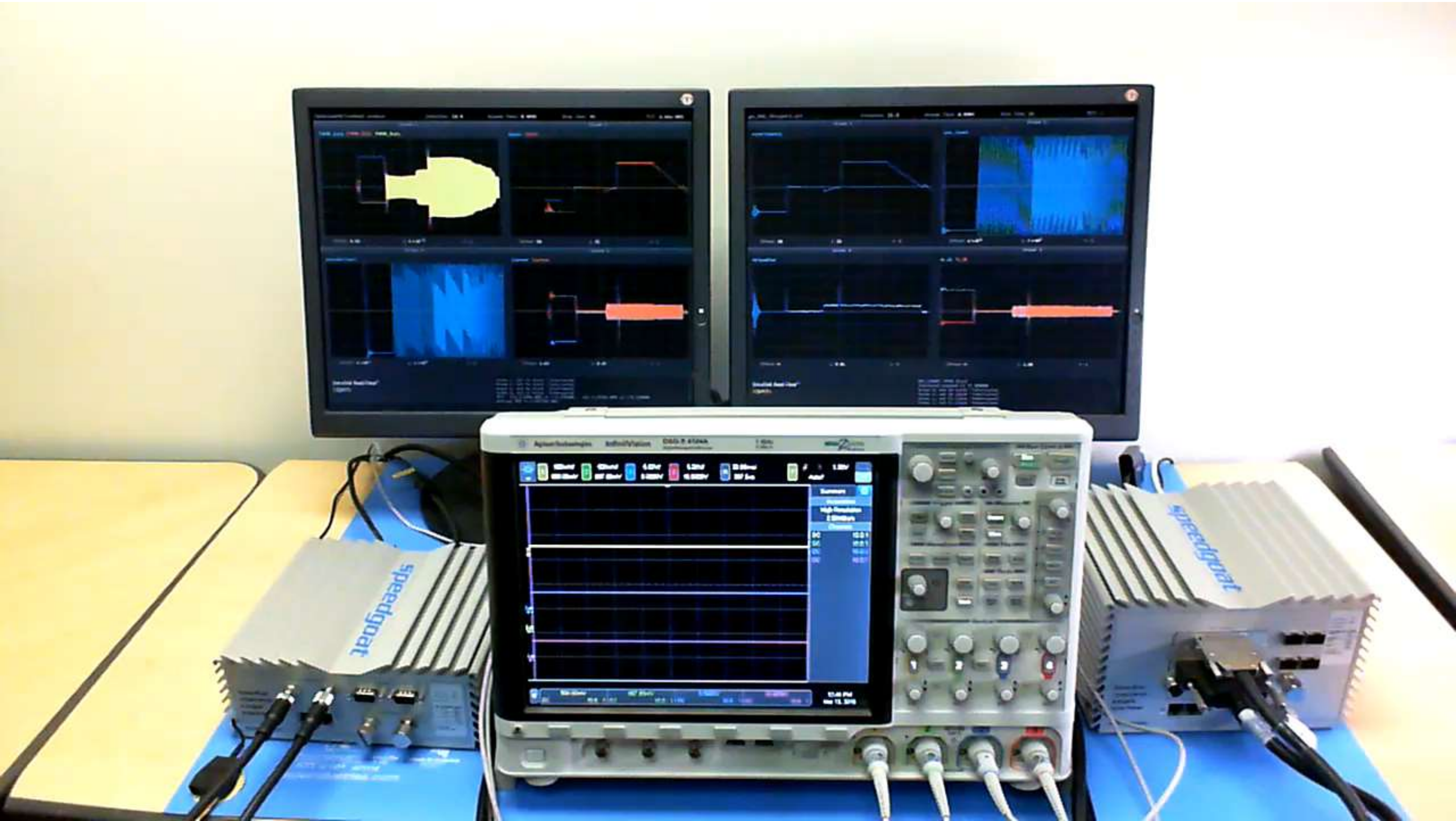
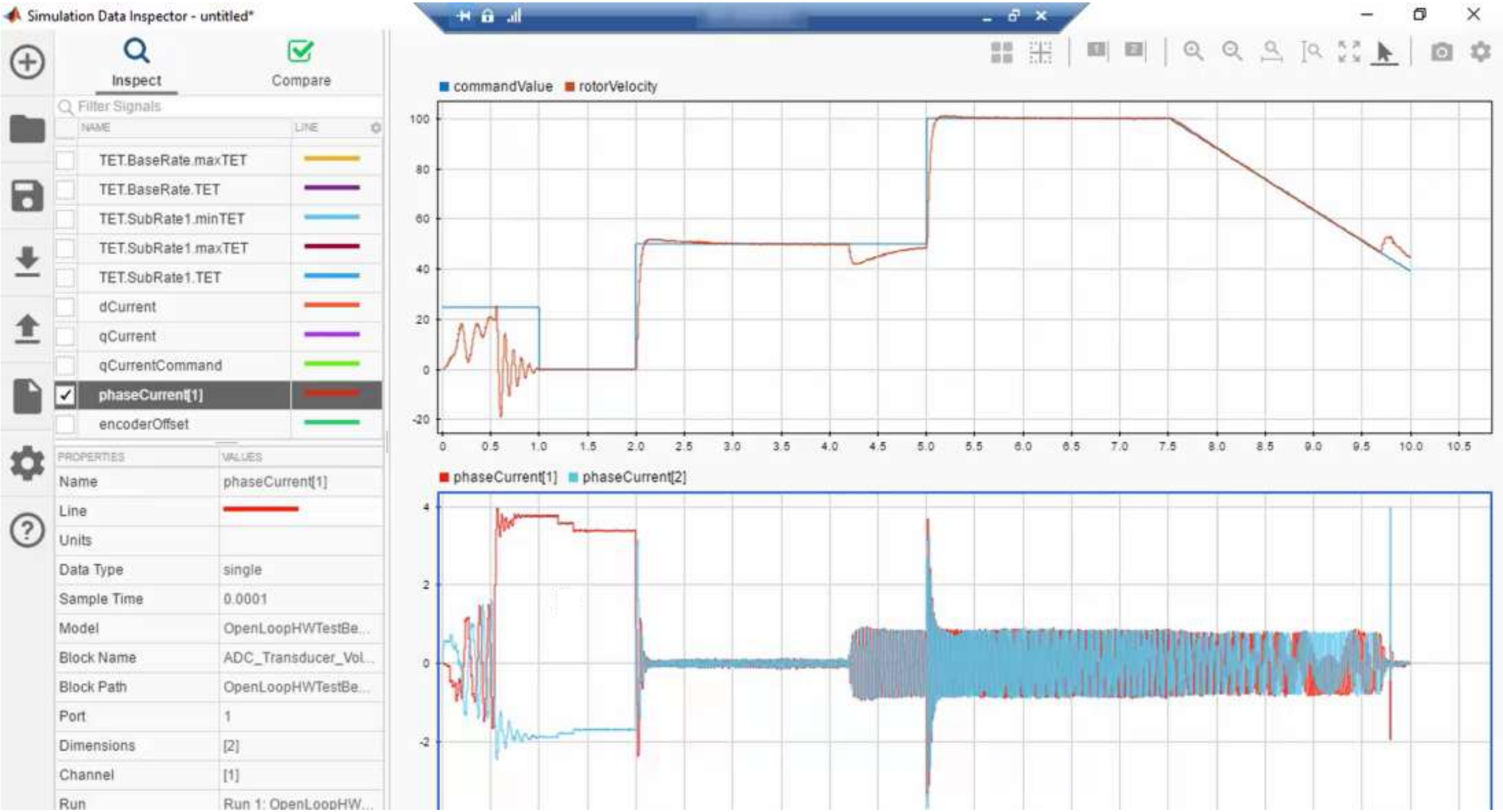
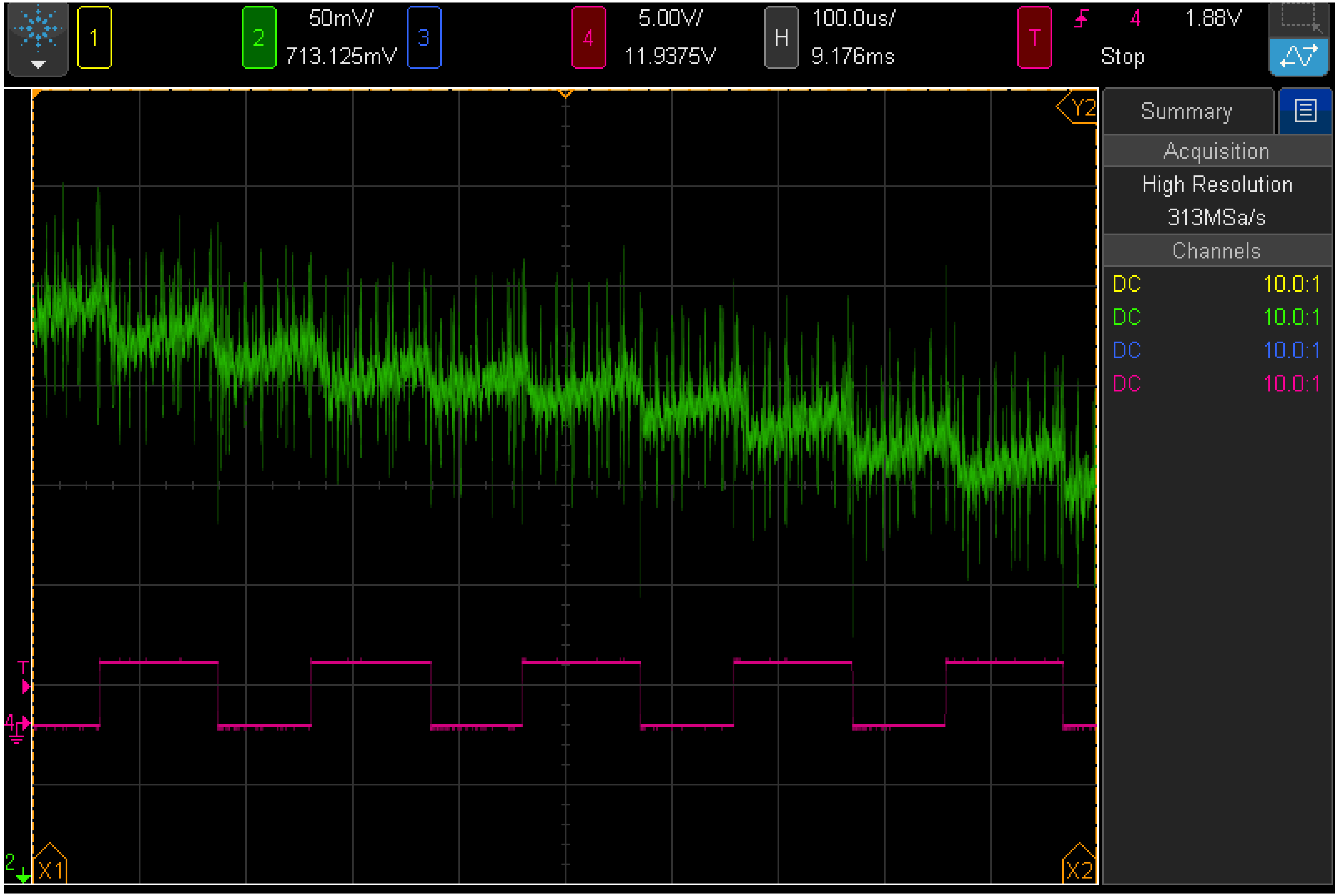
uint16
Calc_CounterValue_Trigger_DA
PCIe_DAC
PCIe_Ideal
Set_TimeStep
Ready


speedgoat
speedgoat

SDI


Simulation Data Inspector - untitled*
Inspect
Compare
Filter Signals
NAME
LINE
TET.BaseRate.maxTET
TET.BaseRate.TET
TET.SubRate1.minTET
TET.SubRate1.maxTET
TET.SubRate1.TET
dCurrent
qCurrent
qCurrentCommand
phaseCurrent[1]
encoderOffset
PROPERTIES
VALUES
Name
phaseCurrent[1]
Line
Units
Data Type
single
Sample Time
0.0001
Model
OpenLoopHWTestBe...
Block Name
ADC_Transducer_Vol...
Block Path
OpenLoopHWTestBe...
Port
1
Dimensions
[2]
Channel
[1]
Run
Run 1: OpenLoopHW...
commandValue
rotorVelocity
phaseCurrent[1]
phaseCurrent[2]

Current Waveforms



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Conclusion

1. Integrate desktop simulation with HIL simulation
2. Native Floating Point support for FPGA
3. Workflow advisor creates a seamless transition from desktop simulation to FPGA implementation

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Want to know more?
Visit us at the booth.

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Simulink Programmable FPGA I/O modules
Optimized for Power Electronics HIL and RCP

The IO334 I/O module is optimized for HIL simulation of real power stages. The card combines fast, low-latency analog and digital I/O capabilities, and is optimized for use with HDL Coder Workflow Advisor from MathWorks.

Analog connectivity:
16 x 5 MHz ADC, +/-10V, ENOB > 13-bit at 5 MHz
16 x 2 MHz DAC, +/-10V, settling time <1us

Multi-Gigabit Transceivers:
4 x MGT for inter-board communication
Enables scalability - I/O and computational resources

Selectable rear plug-ins add:
Digital TTL/RS422 I/O support for PWM / Encoder
Front SFP cages to access MGT at the out side of the enclosure