Simulink for Signal Processing Algorithm Development

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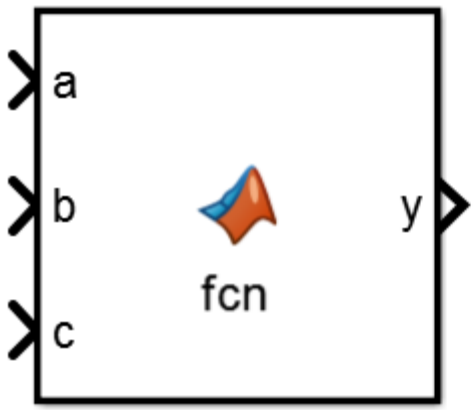
*Use **MATLAB** for algorithm design*

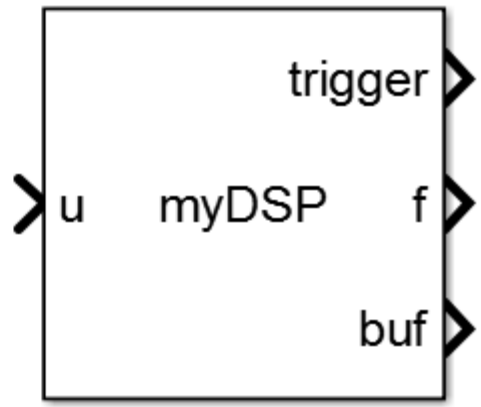
*Use **Simulink** for system design*

DEMO

1. Simulink speaks MATLAB



MATLAB Function

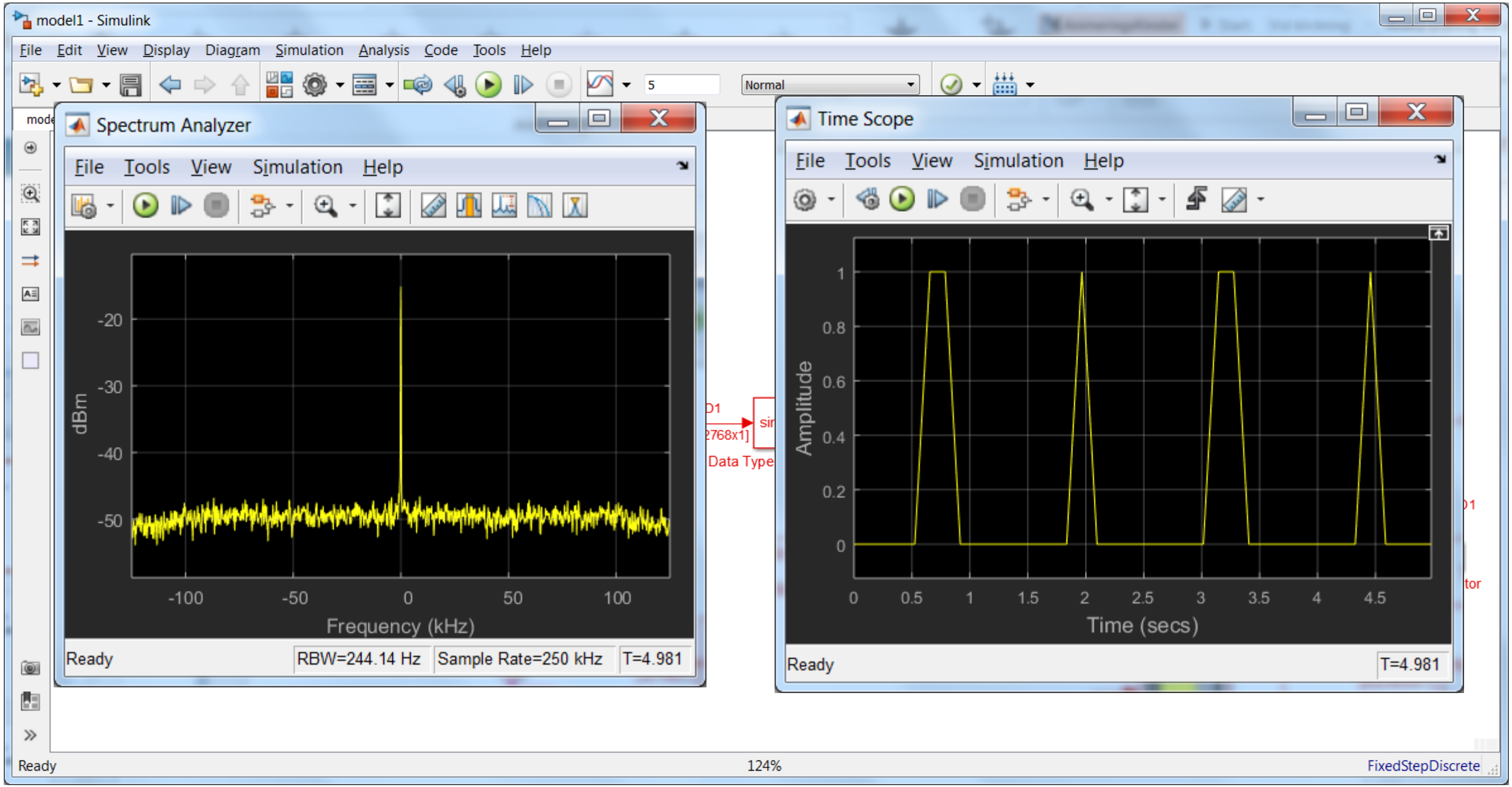


MATLAB System

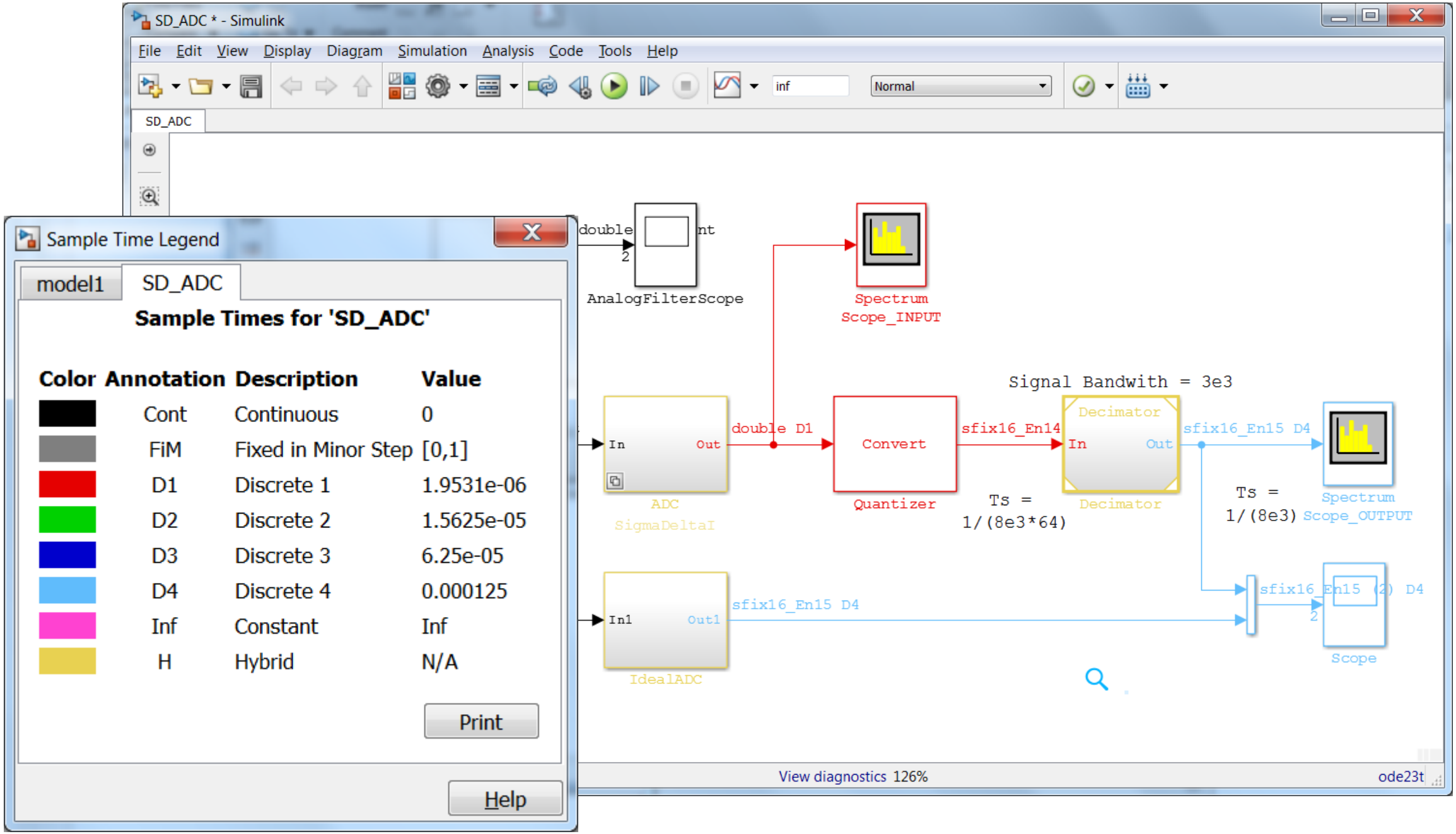
(… and MATLAB speaks Simulink)

```
parfor idx=1:iterations

    simout(idx) = sim(model, 'SimulationMode', 'normal');

end
```

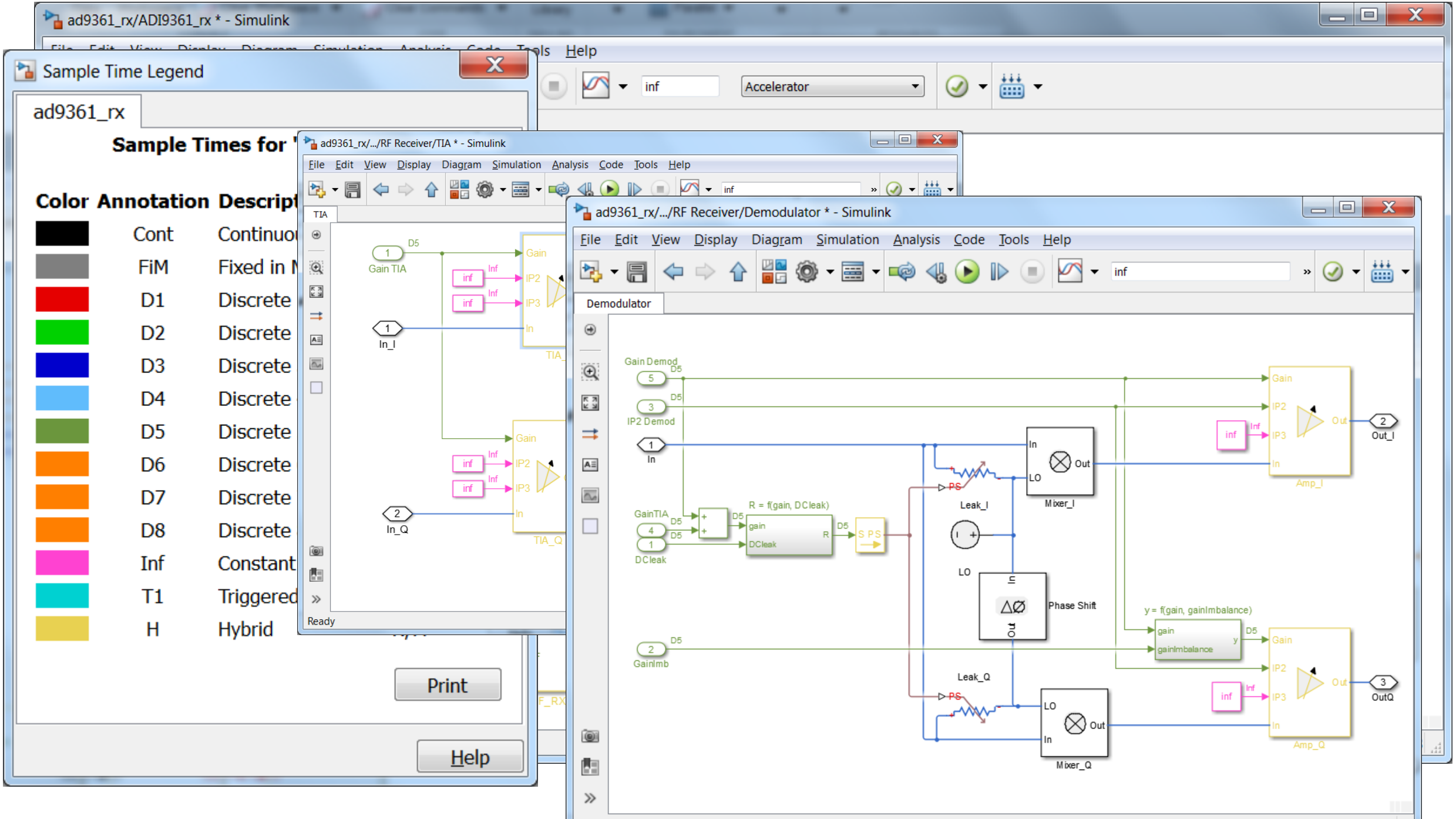
1. **Simulink speaks MATLAB**
2. **Simulink knows what time it is**


model1 - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
Normal
Spectrum Analyzer
File Tools View Simulation Help
-20
-30
-40
-50
dBm
-100 -50 0 50 100
Frequency (kHz)
Ready
RBW=244.14 Hz
Sample Rate=250 kHz
T=4.981
Time Scope
File Tools View Simulation Help
1
0.8
0.6
0.4
0.2
0
Amplitude
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5
Time (secs)
Ready
T=4.981
Data Type
Ready
124%
FixedStepDiscrete

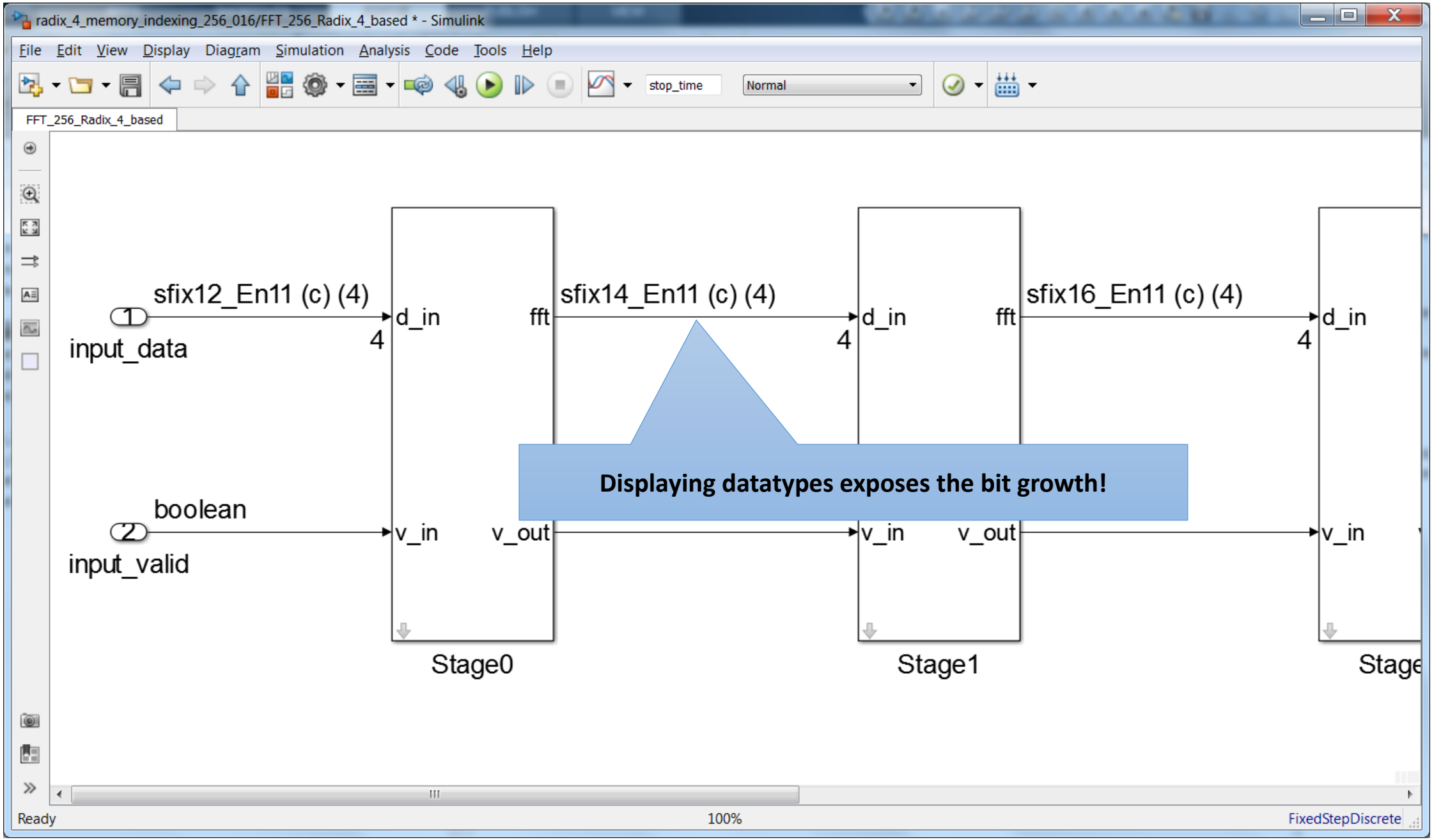
1. **Simulink speaks MATLAB**
2. **Simulink knows what time it is**
3. **Simulink handles multirate systems**


SD_ADC * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
inf
Normal
SD_ADC
double
nt
2
AnalogFilterScope
Spectrum
Scope_INPUT
Signal Bandwith = 3e3
In Out
ADC
SigmaDeltaI
double D1
Convert
Quantizer
sfix16_En14
Ts =
1/(8e3*64)
Decimator
In Out
Decimator
sfix16_En15 D4
Ts =
1/(8e3)
Spectrum
Scope_OUTPUT
In1 Out1
IdealADC
sfix16_En15 D4
sfix16_En15 (2) D4
2
Scope
View diagnostics 126%
ode23t
Sample Time Legend
model1
SD_ADC
Sample Times for 'SD_ADC'
Color Annotation Description Value
Cont Continuous 0
FiM Fixed in Minor Step [0,1]
D1 Discrete 1 1.9531e-06
D2 Discrete 2 1.5625e-05
D3 Discrete 3 6.25e-05
D4 Discrete 4 0.000125
Inf Constant Inf
H Hybrid N/A
Print
Help

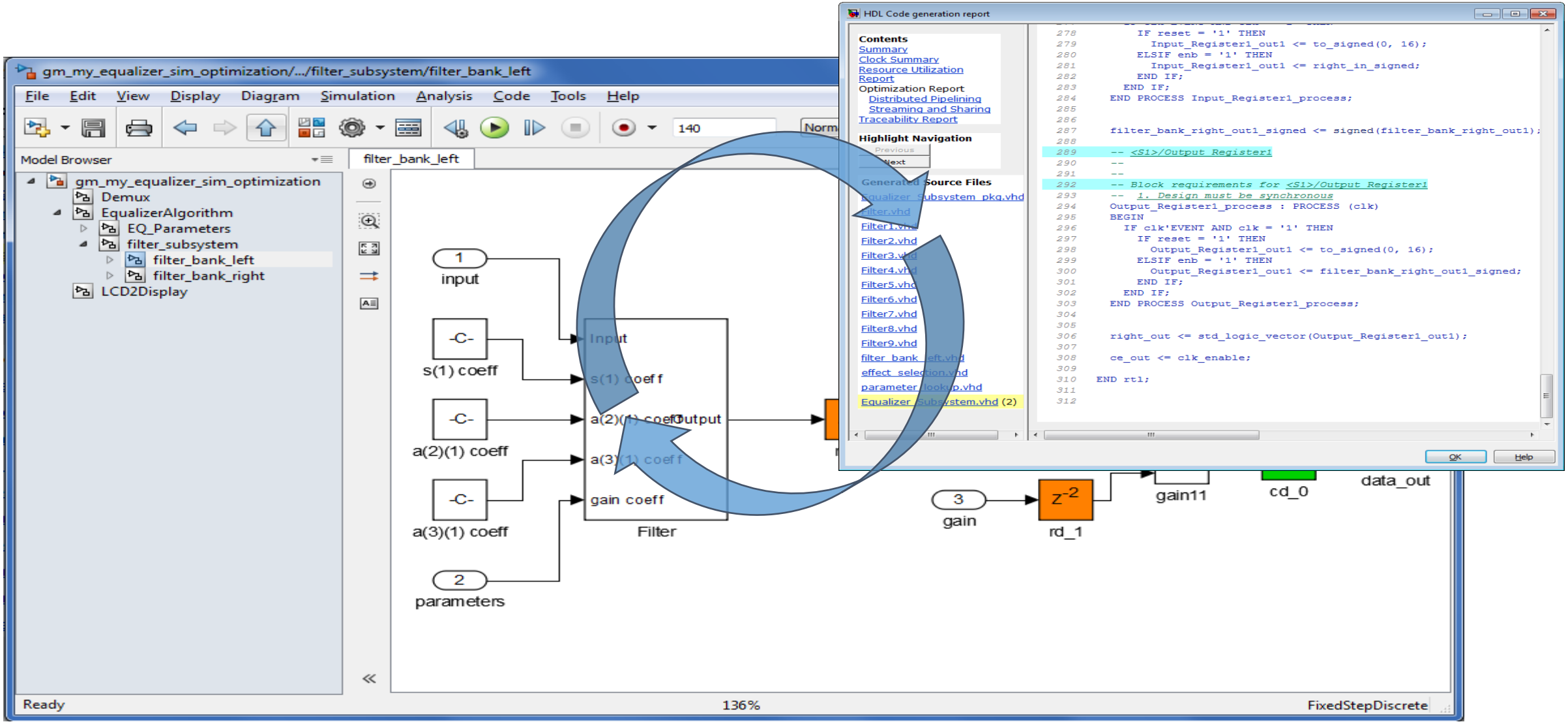
1. Simulink speaks MATLAB
2. Simulink knows what time it is
3. Simulink handles multirate systems
4. Simulink has continuous time


ad9361_rx/ADI9361_rx * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
inf
Accelerator
Sample Time Legend
ad9361_rx
Sample Times for
Color Annotation Descript
Cont Continuo
FiM Fixed in M
D1 Discrete
D2 Discrete
D3 Discrete
D4 Discrete
D5 Discrete
D6 Discrete
D7 Discrete
D8 Discrete
Inf Constant
T1 Triggered
H Hybrid
Print
Help
ad9361_rx/.../RF Receiver/TIA * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
TIA
Gain TIA
In_I
In_Q
Gain
IP2
IP3
In
TIA_I
TIA_Q
Ready
ad9361_rx/.../RF Receiver/Demodulator * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
Demodulator
Gain Demod
IP2 Demod
In
GainTIA
DCleak
R = f(gain, DCleak)
gain
DCleak
R
S PS
Leak_I
Leak_Q
Mixer_I
Mixer_Q
LO
Phase Shift
GainImb
y = f(gain, gainImbalance)
gainImbalance
Amp_I
Amp_Q
Out_I
OutQ
Out

1. Simulink speaks MATLAB
2. Simulink knows what time it is
3. Simulink handles multirate systems
4. Simulink has continuous time
5. Simulink shows datatypes


radix_4_memory_indexing_256_016/FFT_256_Radix_4_based * - Simulink
File Edit View Display Diagram Simulation Analysis Code Tools Help
stop_time
Normal
FFT_256_Radix_4_based
sfix12_En11 (c) (4)
input_data
boolean
input_valid
d_in
v_in
fft
v_out
4
sfix14_En11 (c) (4)
sfix16_En11 (c) (4)
Stage0
Stage1
Displaying datatypes exposes the bit growth!
Ready
100%
FixedStepDiscrete

1. Simulink speaks MATLAB
2. Simulink knows what time it is
3. Simulink handles multirate systems
4. Simulink has continuous time
5. Simulink shows datatypes
6. Simulink maps well to HW/SW arch.


gm_my_equalizer_sim_optimization/.../filter_subsystem/filter_bank_left
File Edit View Display Diagram Simulation Analysis Code Tools Help
Model Browser
filter_bank_left
gm_my_equalizer_sim_optimization
Demux
EqualizerAlgorithm
EQ_Parameters
filter_subsystem
filter_bank_left
filter_bank_right
LCD2Display
1
input
-C-
s(1) coeff
-C-
a(2)(1) coeff
-C-
a(3)(1) coeff
2
parameters
Input
s(1) coeff
a(2)(1) coeff
a(3)(1) coeff
gain coeff
Output
Filter
3
gain
z-2
rd_1
gain11
cd_0
data_out
Ready
136%
FixedStepDiscrete
HDL Code generation report
Contents
Summary
Clock Summary
Resource Utilization Report
Optimization Report
Distributed Pipelining
Streaming and Sharing
Traceability Report
Highlight Navigation
Previous
Next
Generated Source Files
Equalizer_Subsystem_pkg.vhd
Filter.vhd
Filter1.vhd
Filter2.vhd
Filter3.vhd
Filter4.vhd
Filter5.vhd
Filter6.vhd
Filter7.vhd
Filter8.vhd
Filter9.vhd
filter_bank_left.vhd
effect_selection.vhd
parameter_lookup.vhd
Equalizer_Subsystem.vhd (2)
IF reset = '1' THEN
Input_Register1_out1 <= to_signed(0, 16);
ELSIF enb = '1' THEN
Input_Register1_out1 <= right_in_signed;
END IF;
END IF;
END PROCESS Input_Register1_process;
filter_bank_right_out1_signed <= signed(filter_bank_right_out1);
-- <S1>/Output Register1
--
-- Block requirements for <S1>/Output Register1
-- 1. Design must be synchronous
Output_Register1_process : PROCESS (clk)
BEGIN
IF clk'EVENT AND clk = '1' THEN
IF reset = '1' THEN
Output_Register1_out1 <= to_signed(0, 16);
ELSIF enb = '1' THEN
Output_Register1_out1 <= filter_bank_right_out1_signed;
END IF;
END IF;
END PROCESS Output_Register1_process;
right_out <= std_logic_vector(Output_Register1_out1);
ce_out <= clk_enable;
END rtl;
OK
Help