Accelerating the Development of Hardware Testbeds for 5G Wireless Systems

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Hardware testbeds are proven and efficient. They enable engineers to develop and test new technologies and deploy them for limited field trials. During the development and deployment of 4G LTE technologies, Ericsson and other leading base station vendors utilized testbeds extensively to accelerate the speed of time-to-market and demonstrate technology leadership, while keeping the design teams small and agile. As the development of next generation of 5G wireless technology gains momentum, engineering teams are using the best practices and lessons learned from the 4G LTE experience. In particular, they are extending the use of testbeds to accelerate the development and field-testing of 5G algorithms and system architectures.

FPGA-based prototyping hardware are the preferred and practical platform for developing and deploying testbeds in the field. Most R&D teams specialize in advanced wireless communications algorithms but do not have the requisite expertise or time to deploy the algorithms on FPGA hardware. In this article, we describe an integrated methodology and workflow for the development of advanced algorithms and rapid deployment to hardware testbeds, and their usage in engineering the next generation of wireless communication systems.

Introduction

5G wireless technology is currently under active research and development. When fully deployed, 5G is expected to provide numerous advantages, including gigabit data rates, ubiquitous coverage, ultra-low latency, and improved connectivity for connected vehicles as well as machine-to-machine (M2M) and Internet of Things (IoT) applications. Modulation schemes, beamforming techniques, millimeter wave technology, and MIMO architectures are expected to be significantly different from the current 4G technologies. Standards are yet to be ratified, and companies and organizations that are in a position to influence the standardization process by demonstrating technical leadership and readiness will seize a market advantage.

Based on the experience of bringing 4G technologies to market and influencing the standardization of LTE, LTE-A, and related standards, companies have realized the value of rapid design iterations and placing proof-of-concept prototypes in field trials quickly. Testbeds employed as flexible and reconfigurable design platforms have proven to be dependable and efficient for the rapid design and verification of new concepts, as well as for their deployment in pre-commercial field trials.

Hurdles in Getting to Market First

Testbeds are ideally suited for demonstrating new technology, creating proofs-of-concept, deploying pre-commercial prototypes, and showcasing new technology to demonstrate market readiness or technology leadership. Companies involved in 4G LTE development learned firsthand the importance of being first to market. During the field trial stage, companies are engaged in a race against time and their competition. Optimizations for power consumption, FPGA area, or even cost are less critical compared to the engineering team's development speed.

When working on 5G wireless technologies, or indeed any emerging technology, system engineers and architects must focus on accelerating research and innovation, and minimize the valuable engineering time and resources spent on programming, debugging software, or building FPGA hardware realizations of their design ideas. This is particularly important when working with fast-changing

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pre-standardization communication protocols. The tools and workflows that interface to testbeds must support rapid design iterations and rapid deployment of new algorithms or design changes.

One significant hurdle for many teams is a lack of experience with FPGA development workflows and RTL implementation of signal processing and communications algorithms. For a typical R&D group that consists of engineers with strong signal processing and wireless communications algorithm development backgrounds but relatively little experience with hardware implementation, it is often difficult to implement FPGA-based radio prototypes and testbeds without outside assistance.

"The main challenge is to implement FPGA based radio signal processing in a small team mainly consisting of people with signal processing and programming background."

—Tomas Andersson, Ericsson

The group has two options: assemble a new team that focuses on hardware implementation (FPGA or DSP) or enlist other hardware and software groups within their organization.

Even when another engineering group provides assistance, delays are inevitable if that group uses a traditional process. It takes time to manually convert candidate algorithms written in floating point C or MATLAB® into fixed point equivalents, and then to perform a second conversion into synthesizable HDL code. Each stage adds significant design and verification cost.

An Integrated Workflow for Shortening Time-to-Market

For most R&D teams, the key hurdles are the lack of specialized expertise in FPGA and hardware implementation, and delays and inflexibility of traditional development processes.

An integrated workflow for system design with MATLAB and Simulink® can overcome these challenges (Figure 1). By developing fixed point-algorithms directly in MATLAB and Simulink, and verifying them in system-level simulations, R&D engineers can rapidly iterate on new design concepts. Once the algorithm runs correctly in simulation, the engineers can automatically generate synthesizable Verilog or VHDL code for deployment to an FPGA based testbed with the click of a button.
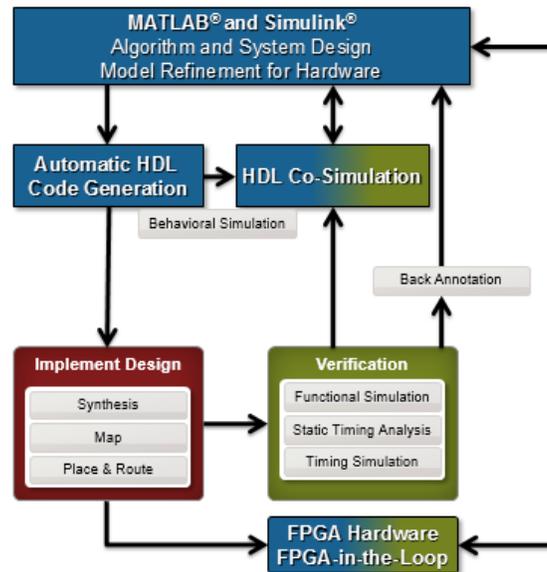
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Figure 1. Integrated workflow from system design to hardware with MATLAB and Simulink.

Next, we will consider the workflow utilized by Ericsson for rapid and field test deployment of hardware testbeds for prototyping new communication standards as a case study.

Case Study: Hardware Testbeds at Ericsson

In addition to providing leadership in radio communication standards organizations, the Systems and Technology group at Ericsson works on standardization, concept development, and radio technology strategy. The group uses hardware testbeds to achieve several strategic objectives including early demonstration of new capabilities, completion of proof-of-concept projects, and the development and deployment of pre-commercial prototypes. Through these activities, the group helps Ericsson showcase new technologies and capabilities and achieve first-to-market technology leadership.

In the past, the group's system engineers or architects developed floating-point algorithms, using MATLAB to explore new design concepts. While this approach was useful for rapidly validating concepts on the desktop, the group experienced many of the hurdles cited above when they sought to move from testing on the desktop to testing in the field with real hardware. As a first step in overcoming these hurdles, the group decided to design algorithms directly in fixed point. To simplify this often difficult task, they adopted Simulink, Communications System Toolbox™, DSP System Toolbox™, and Fixed-Point Designer™ as their fixed-point design platform. Ericsson engineers implement detailed algorithms within subsystems to simplify the visual representation of the design and raise the abstraction level of the top-level model. Using subsystems in this way enables the engineers to readily explain their design and methodology to senior management and customers, while maintaining the fidelity of the underlying hardware design. For example, engineers use MATLAB for control logic such as Symbol RAM Read Control or Window Add and Pass-through, and for common signal processing functions. They incorporate the MATLAB code directly into the overall Simulink model of the LTE Modulator (Figure 2).
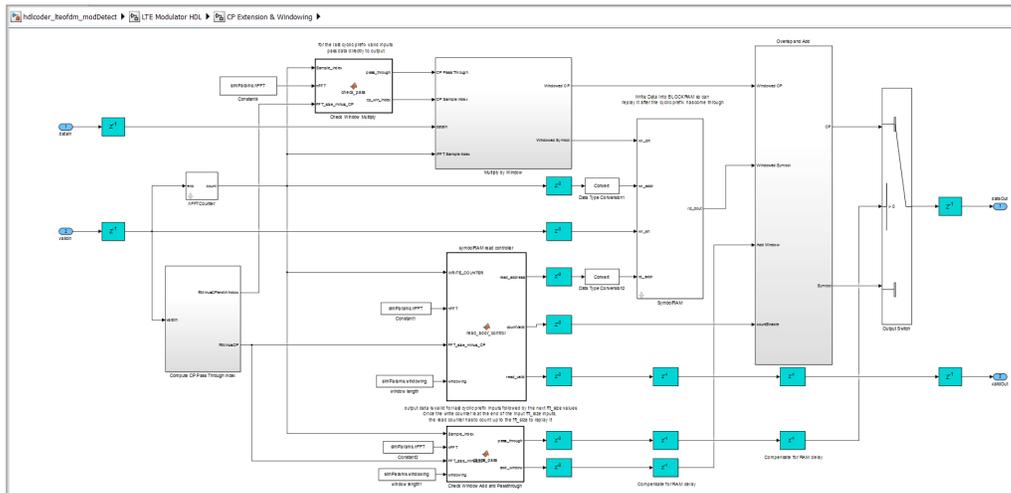
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Figure 2. Using MATLAB algorithms and logic in a Simulink model of an LTE Modulator.

Now that they have switched to Model-Based Design, Ericsson's engineers use one model for both simulation and implementation on the FPGA prototype; they no longer need to maintain two different representations of the same design. In addition, they no longer need to handoff the system design to specialized hardware prototyping teams for implementation. The models are ready for FPGA implementation at any time because the group draws from a library of fixed-point algorithm blocks that support automatic HDL code generation with HDL Coder. They have found that when the simulation works, then the automatically generated HDL code will work on the FPGA. As a result, the team has short design iterations and can rapidly implement design changes for timing closure or to accommodate changes in the standards or specifications.

"When a new design is required because a new design idea emerges, using HDL coder, we were able to demonstrate that the change was acceptable and have a working demonstration in less than one week." —Tomas Andersson, Ericsson

To complete and deploy a full proof-of-concept on a hardware testbed, the group integrates algorithms developed with MATLAB and Simulink with other system components in a standard FPGA development environment. Specifically they integrate HDL code automatically generated from Simulink using HDL Coder with manually coded custom interfaces and IP cores from FPGA vendors for components such as soft processors, DMA, and physical interfaces. When changes are required, the engineers make the change in Simulink, regenerate the code (typically within minutes), integrate the code in the FPGA development environment, and synthesize it for FPGA implementation. Ericsson engineers have noted that the generated code is well structured, readable, and functionally accurate.

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Conclusion

For most R&D teams that are working on the next generation wireless algorithms, the key hurdles are the lack of specialized expertise in FPGA and hardware implementation, and delays and inflexibility of traditional development processes.

An integrated workflow for system design with MATLAB and Simulink enables engineers with algorithm design expertise but limited hardware experience to create and deploy hardware testbeds. Such workflows are particularly suited for prototyping and proof-of-concept projects with tight design schedules. Engineers are no longer solely dependent on specialized hardware experts or scarce implementation teams. Compared to a traditional process, this approach has several advantages. Using a single model for simulation and code generation greatly simplifies the process and eliminates hand-offs between system design and implementation teams. Further, once the model verified via simulation, it is ready for FPGA implementation. Iteration cycles for design changes are much shorter, enabling the engineering team to respond quickly to changes in specifications or standards.

For wireless system design and hardware prototyping see an overview of *wireless system design capabilities* and *HDL integrated workflows*. For further information on using HDL Coder see the *HDL code examples*. To learn more about how Ericsson engineers used hardware testbeds, watch their presentation on *radio testbed design using HDL Coder*.

In addition to *Ericsson*, several worldwide market leaders including Huawei, *Qualcomm*, *Broadcom*, *Bosch*, *Renesas*, *Philips Healthcare*, and others have adopted MATLAB, Simulink, HDL Coder, and HDL Verifier for prototyping, implementing, and verifying ASIC and FPGA implementations of advanced communications, electronics, and semiconductor systems.

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