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Study of the tracking of FHSS signal over AWGN channel

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ABSTRACT

Frequency Hopping Spread Spectrum (FHSS) communications utilizes a pseudo random code to spread the bandwidth of the data being transmitted over a much wider range than is required by the data. Due to the pseudo random nature of the carriers selected for transmission, the spreading and despreading process must occur simultaneously to recover the transmitted data signal. This requires the receiver have knowledge about the instant the transmitter began transmitting and the propagation delay between the two. However, in real world systems, this information is unavailable to the receiver. The paper utilizes MATLAB Simulink to demonstrate a method of synchronizing the code clock at the receiver with the code clock at the transmitter. This fine alignment process is known as code tracking.

KEYWORDS

FHSS system, tracking method, AWGN channel

1. INTRODUCTION

Spread spectrum communications refers to the technique of taking an information bearing signal of a particular bandwidth and deliberately spreading it out on the frequency domain such that the signal now occupies a much wider bandwidth [1, 2].

There are three main techniques utilized in spread spectrum communications: direct sequence spread spectrum, frequency hopping spread spectrum, and time hopping spread spectrum. With each utilizing a code that is pseudorandom in nature to achieve the spreading [3, 4].

Each system of spreading the spectrum requires a method of recovering the transmitted signal. This requires the receiver to recover the spreading code timing from the received signal. The acquisition system brings the receiver and transmitter code sequences into coarse alignment while tracking the system [5, 6].

The paper concentrates on demonstrating a means of code tracking on Frequency Hopping Spread Spectrum (FHSS) systems. The tracking deals with correction of timing offsets and frequency offsets of the clock running the code generators [7]. Although acquisition is an essential first step before tracking can commence, there is no in depth treatment of acquisition methods. This is because the scope of the paper is to design and demonstrate a code tracking method. Subsequently only the simplest acquisition system is utilized.

2. DESIGN PROCEDURE

2.1. Simulation model

The tracking system is implemented using MATLAB Simulink. The complete model overview is shown in Fig. 1, with each block explained in the following subsections.

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2.1.1. Transmitter. This subsystem contains the binary data input, 2-frequency shift keying (2-FSK) modulator, the pseudonoise (PN) generator, and the hopping carriers. The Transmitter subsystem is shown in Fig. 2.

2.1.1.1. Bernoulli binary generator. This block is used to provide the digital data input. It is set to a rate of 1kbps and the 1 and 0 are equally likely to occur.

2.1.1.2. 2-FSK_mod. This block implements the 2-FSK modulation scheme utilizing a set of two oscillators as shown in Fig. 3

The separation frequency is 2 kHz which obeys the orthogonality condition. A binary 0 is represented by 10 kHz and a binary 1 is represented by 12 kHz.

2.1.1.3. Transmit_mix. This block carries out the mixing operation and it is implemented using the MATLAB product block.

2.1.1.4. Transmitter_clock. This subsystem contains the clock that drives the PN generator for the transmitter. The subsystem contains the voltage controlled clock (VCC) that runs at 500Hz meaning the system transmits two symbols per hop and is hence a slow frequency hopping (SFH) system.

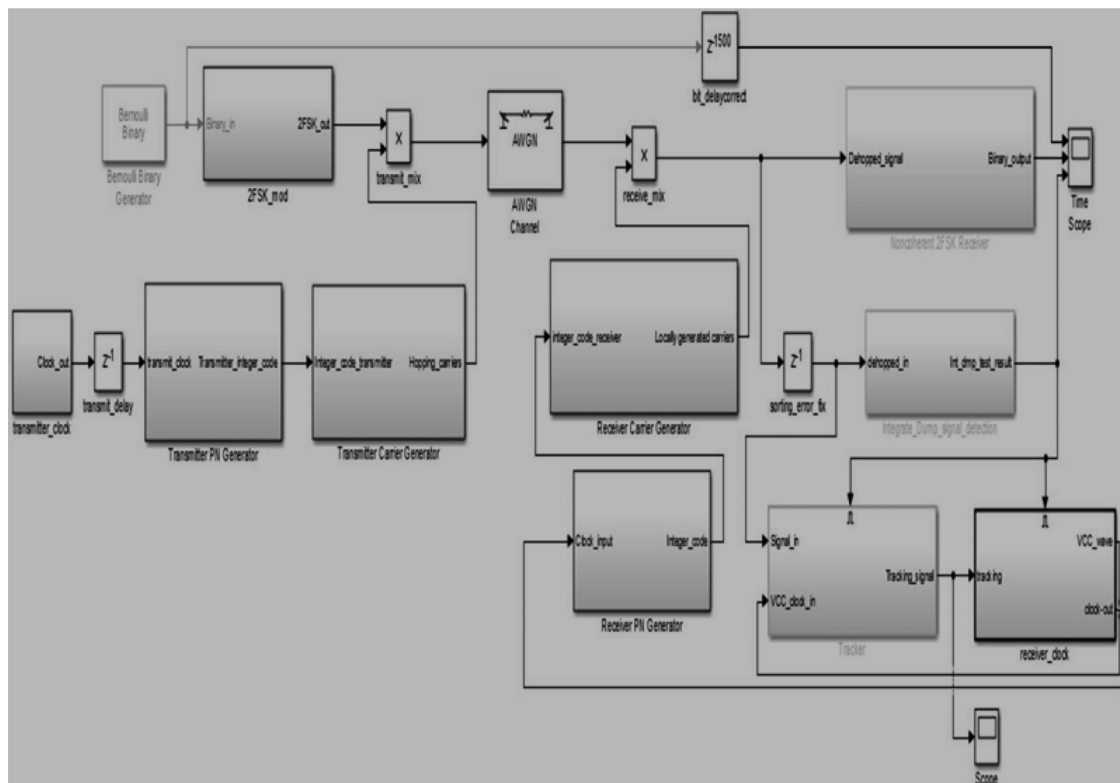


Figure 1. System block diagram

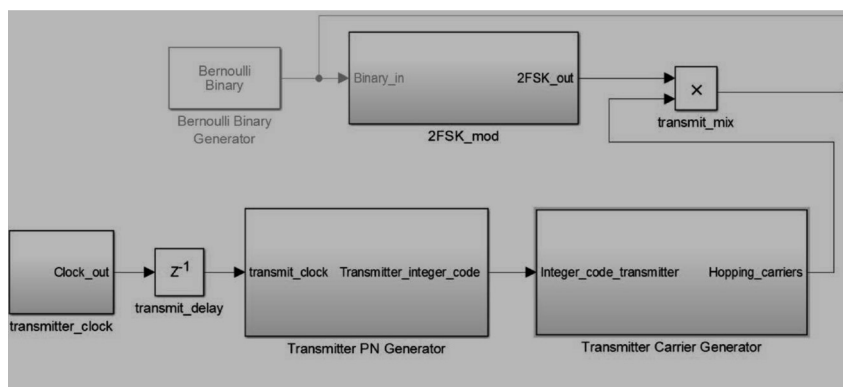
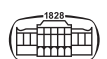


Figure 2. Transmitter block diagram



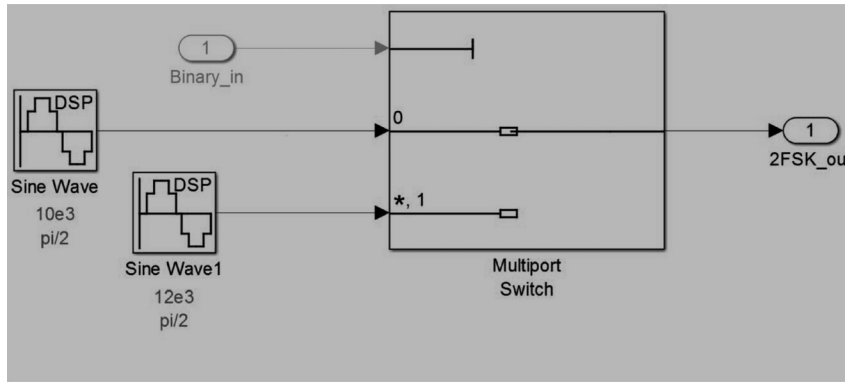


Figure 3. 2-FSK modulator

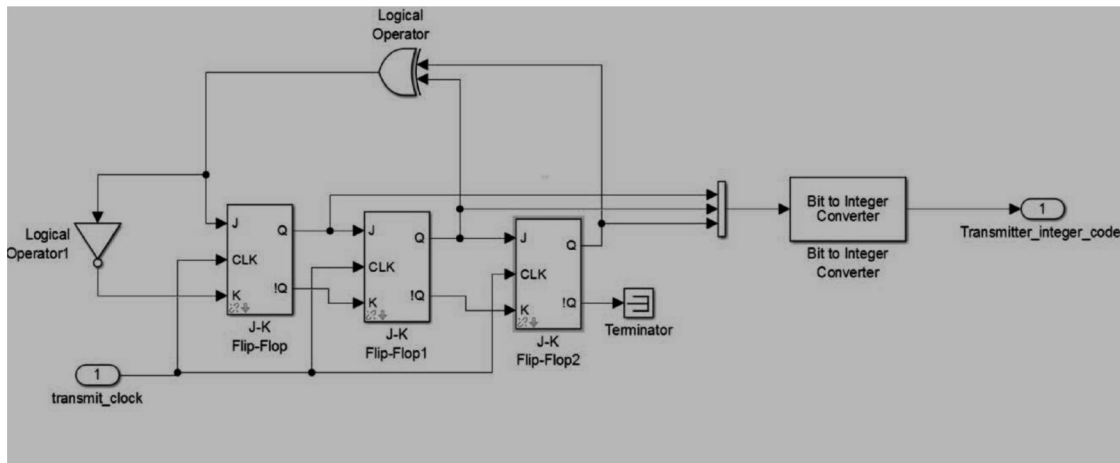


Figure 4. Transmitter PN sequence generator

2.1.1.5. Transmitter PN generator. This subsystem, which is shown in Fig. 4, contains the flip flops required to implement the pseudo noise sequence. The implementation is done using JK flip flops interconnected to behave as D flip flops. The feedback polynomial is $x^3 + x^2 + 1$ and the initial

seed is 100. The resulting sequence is a maximal length sequence of period 7. The implementation is a 3 stage linear feedback shift register (LFSR). The bit to integer converter is used by the next transmitter carrier generator subsystem to generate the hop set.

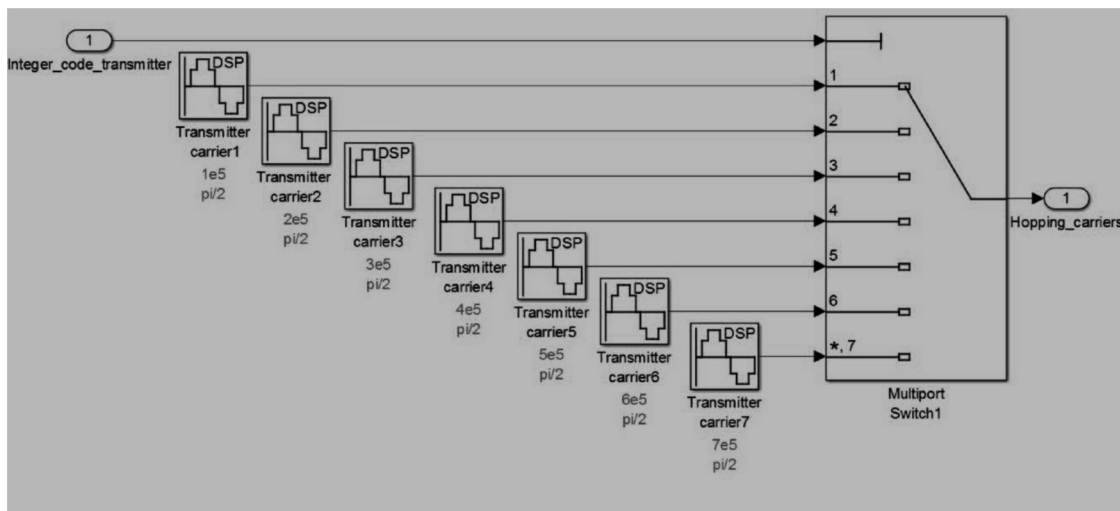


Figure 5. Transmitter carrier set generator

2.1.1.6. Transmitter carrier generator. This subsystem, shown in Fig. 5, generates the hop set. The hopping carriers range from 100 kHz to 700 kHz in steps of 100 kHz, which is an integer multiple of the 2-FSK frequency separation and the input bit rate.

2.1.1.7. Transmit delay. This block is a delay block that performs the job of timing correction to correct for the PN generator being positive edge triggered. Its value is set to 1 to have minimal effect on the timing of the signal.

2.1.2. AWGN channel. The channel is modeled as an AWGN, which is an additive white Gaussian noise channel. This models the channel as having corrupting noise being added to the signal in the process of transmission.

2.1.3. Receiver. The receiver subsystem overview is shown in Fig. 6

2.1.3.1. Receive mix. This block utilizes the MATLAB product block to model the de-hopping operation by multiplication by the locally generated hop set.

2.1.3.2. Receiver carrier generator. This subsystem contains the locally generated hop set and is identical to the transmitter carrier generator (Fig. 5).

2.1.3.3. Receiver PN generator. This subsystem generates the maximal length PN sequence and its construction is identical to the PN generator at the transmitter (Fig. 4).

2.1.3.4. Sorting error fix. This MATLAB block uses a delay of 1 integration period to force the acquisition and tracking systems to activate after signal is received. The primary purpose of the block is to prevent ambiguous execution errors occurring in the model.

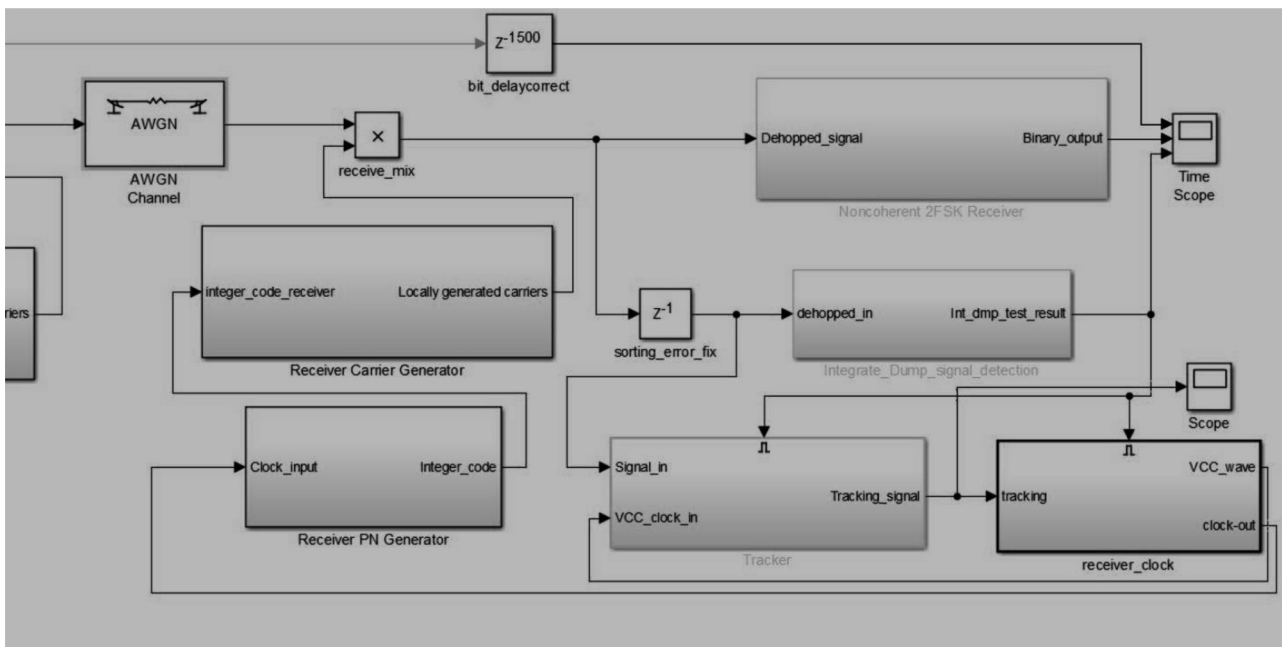


Figure 6. Receiver block diagram

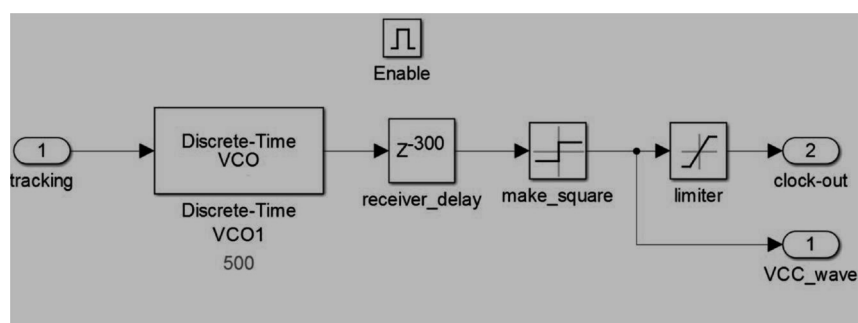
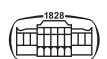


Figure 7. Receiver clock



2.1.3.5. Receiver_clock. This clock controls the PN generator for the transmitter. This subsystem is constructed as shown in Fig. 7.

2.1.3.6. Noncoherent 2-FSK receiver. This subsystem, shown in Fig. 8, performs the task of recovering the original binary information sequence from the received symbols of waveforms of 10 kHz and 12 kHz.

This receiver does not utilize any phase information from the incoming signal and hence it is noncoherent. The conditional switch functions as the decision algorithm to output a binary 1 or 0 dependent on which arm has the larger output. The integration period of the integrate and dump filter is set to the symbol period which is equivalent to

the input data bit rate. The comparison between the two arms is performed by the Subtract1 block.

2.1.3.7. Integrate_dump_signal_detection. This subsystem, which is shown in Fig. 9, performs the serial search operation of the receiver as well as enabling the tracking subsystem and receiver clock subsystems.

The integrate and dump filters are utilized as matched filter energy detectors to detect the presence of successfully dehopped signal. Once the signal level crosses the preset threshold, this subsystem enables the receiver clock and the tracking subsystem. The system waits on one of the channels for the signal to be detected indicating the received signal has been dehopped. The transmitter has knowledge of the

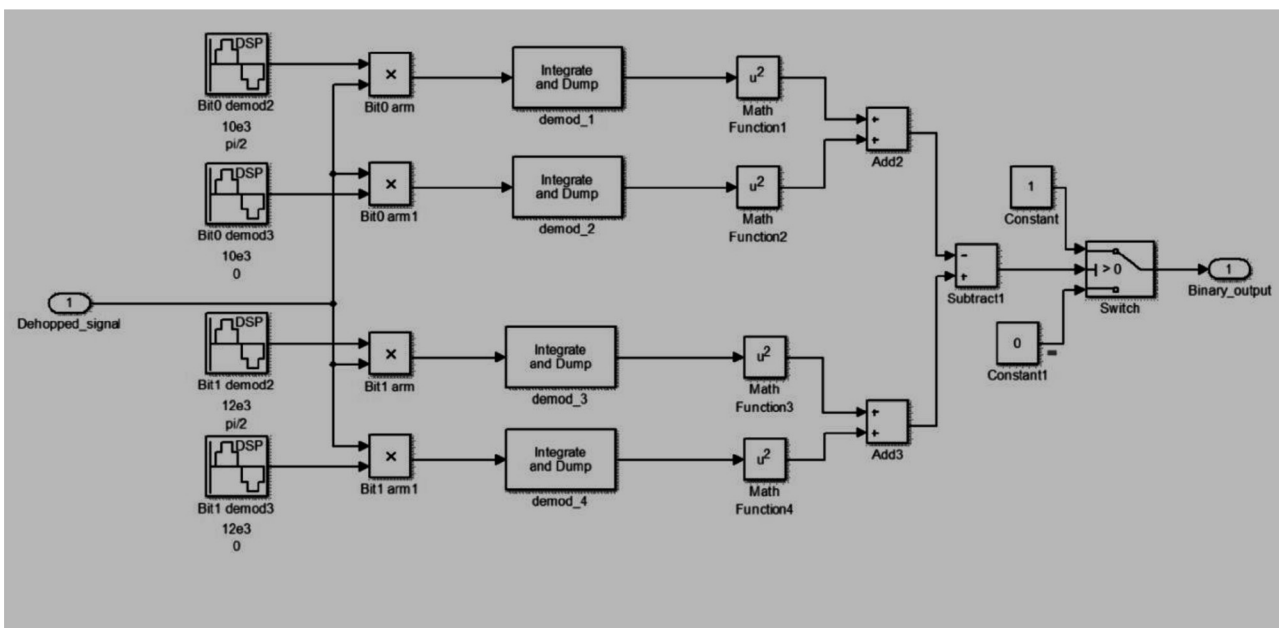


Figure 8. Non-coherent 2-FSK demodulator

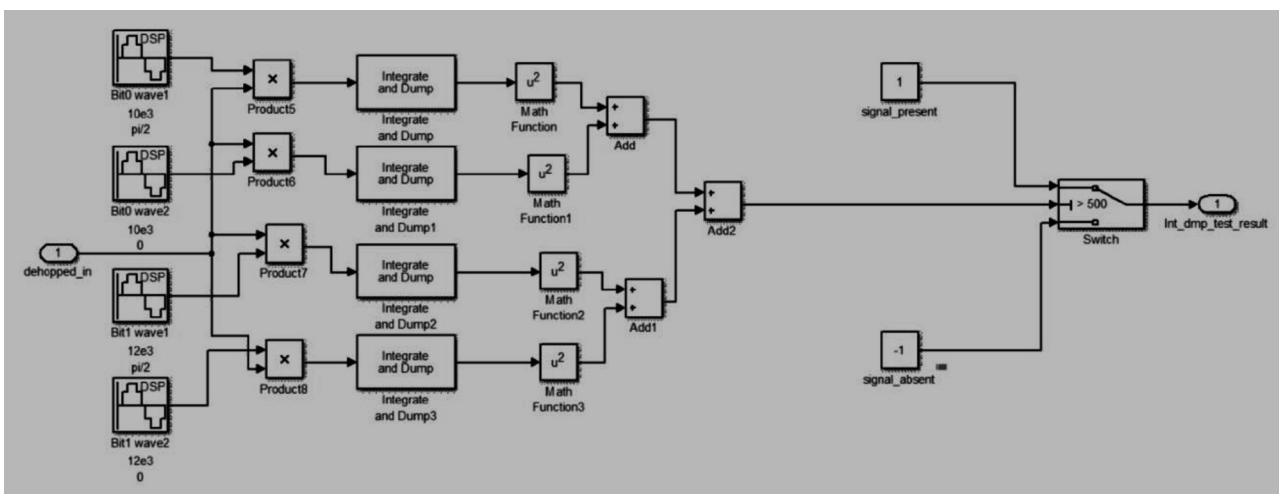


Figure 9. Signal detection circuit utilizing integrate and dump filters

hopping carriers and the hopping sequence and simply initiates the clock to start following the hopping pattern.

to control the frequency of the VCC in the receiver clock subsystem.

2.1.3.8. Tracker. This subsystem implements the tracking operation. It is modeled as an enabled block that is dependent on the signal being acquired first before initiating the tracking of the signal to correct for timing offset. The block diagram of the subsystem is shown in Fig. 10 below. The Lowpass filter is used to extract the mean of the tracking signal, which is used

2.1.3.9. Matched_filter_energy_detector. This is a subsystem within the tracker that is used to detect the timing errors between the receiver and transmitter clocks. It has a higher sensitivity than the signal detector used to serial search the incoming signal during acquisition. The energy detector detects misalignment between the received hopping

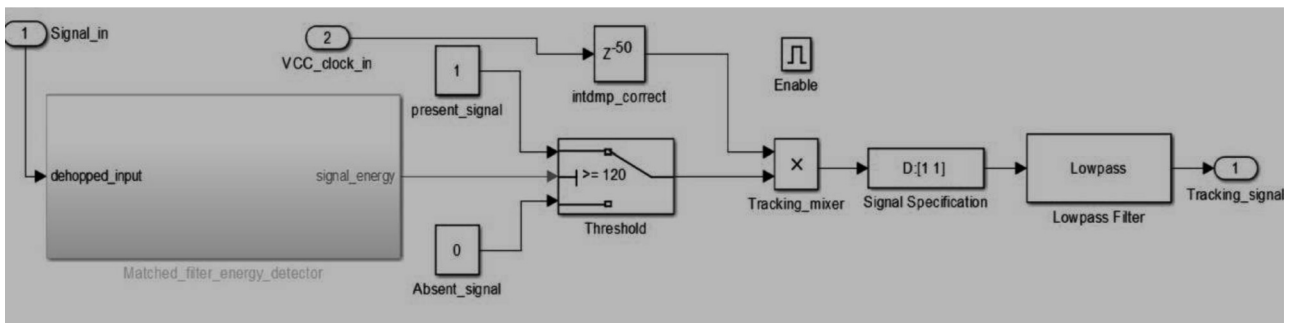


Figure 10. Tracking subsystem

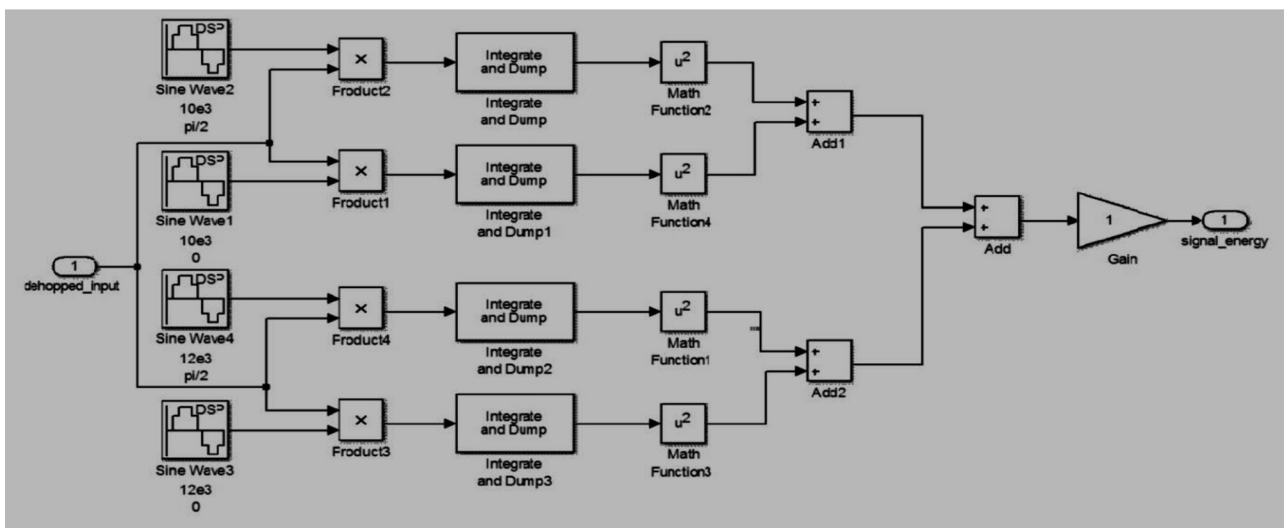


Figure 11. Sensitive matched filter energy detector

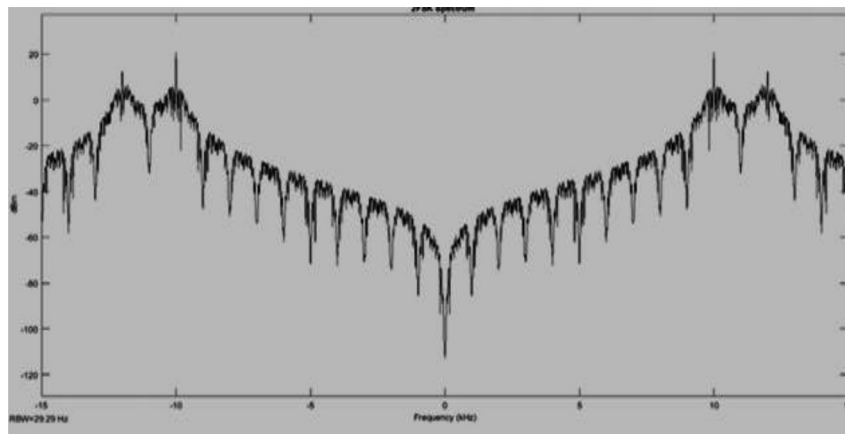
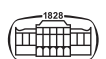


Figure 12. Spectrum of 2-FSK modulated binary input



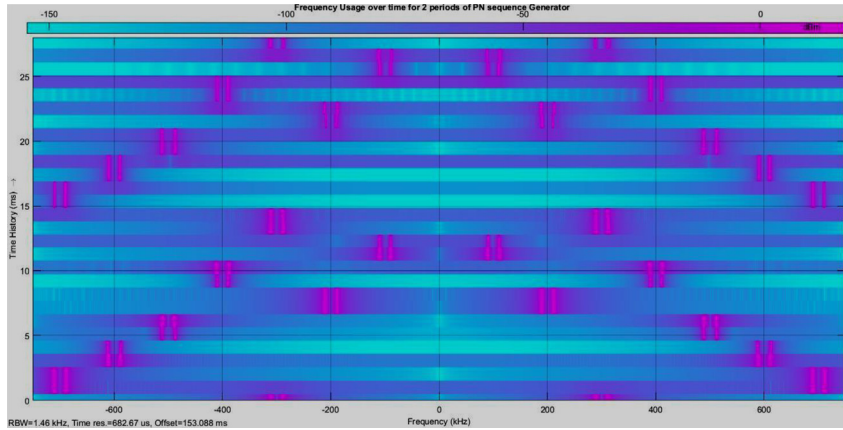


Figure 13. Spectrogram showing spectral occupancy of carriers

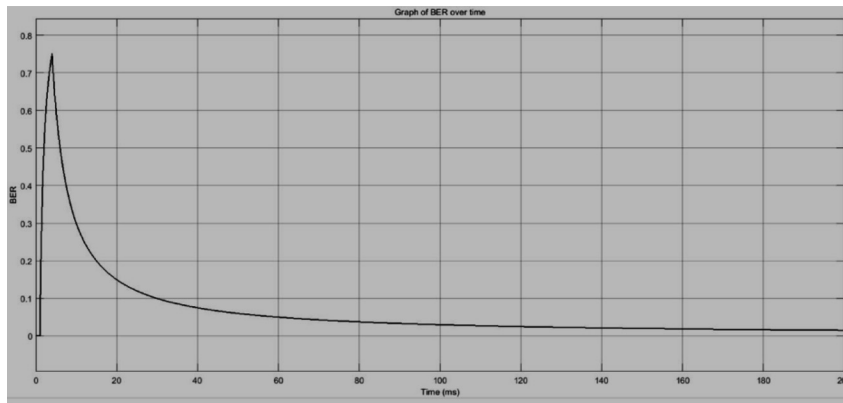


Figure 14. BER change over time

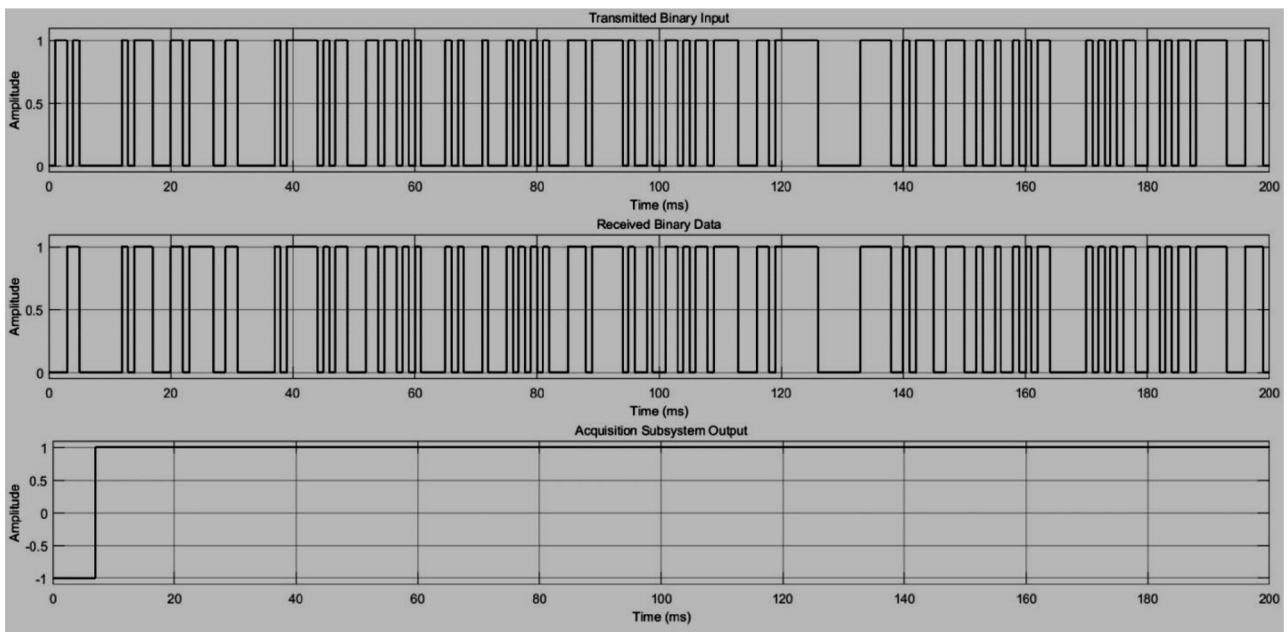


Figure 15. Transmitted binary, received binary and acquisition subsystem output



pattern and the locally generated hopping pattern. The subsystem is shown in Fig. 11.

3. RESULTS

3.1. Modulation and spreading

The modulation method used to convert the digital input to two distinct frequencies utilized a pair of oscillators and the spectrum of the 2-FSK signal is shown in Fig. 12. The two

peaks of 10 kHz and 12 kHz correspond to binary 0 and 1, respectively.

The result of the signal being spread out is shown by the spectrogram below in Fig. 13. The dark line segments indicate the frequency is being utilized to transmit data over the channel. The range of carriers is from 100 kHz to 700 kHz.

3.2. Transmission over the channel

The AWGN channel is utilized to demonstrate that the system designed is successfully transmitting data and receiving. Fig. 14 shows the results with the AWGN

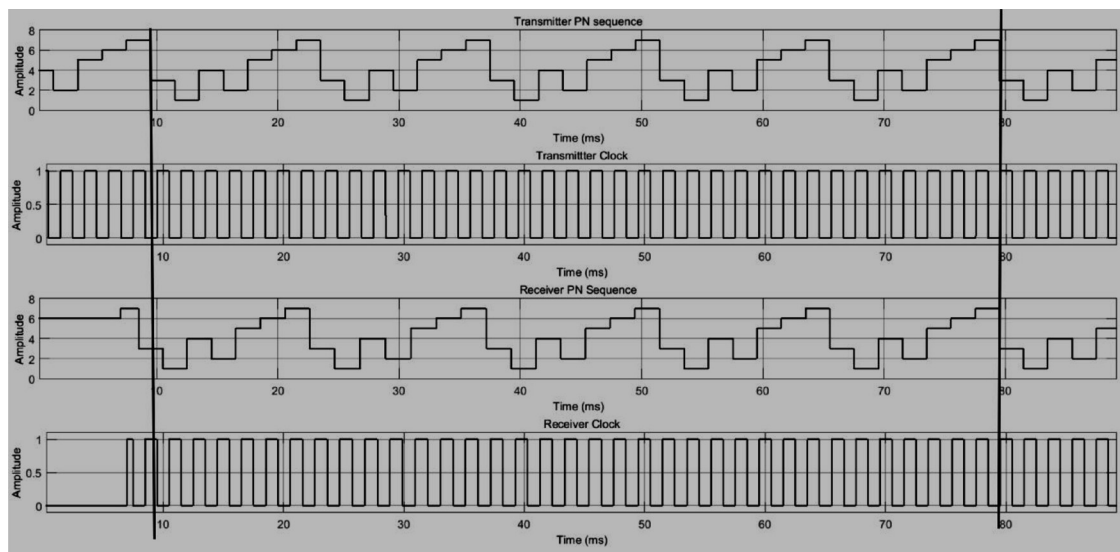


Figure 16. Receiver PN sequence leading transmitter, alignment improvement highlighted by reference lines

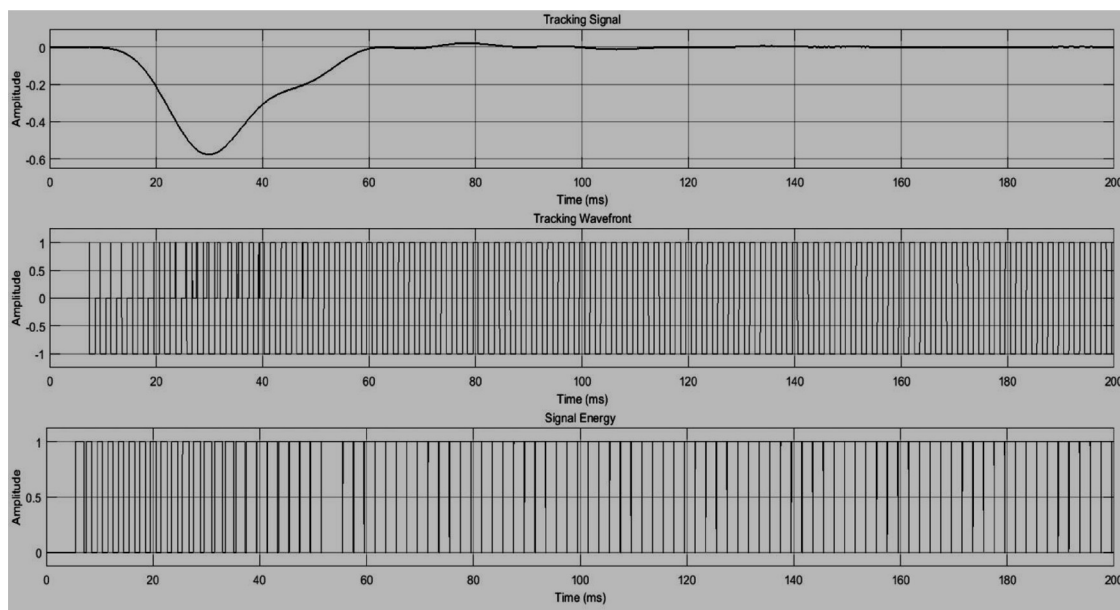
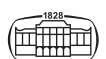


Figure 17. Tracking signals with receiver hopping pattern leading transmitter hopping pattern



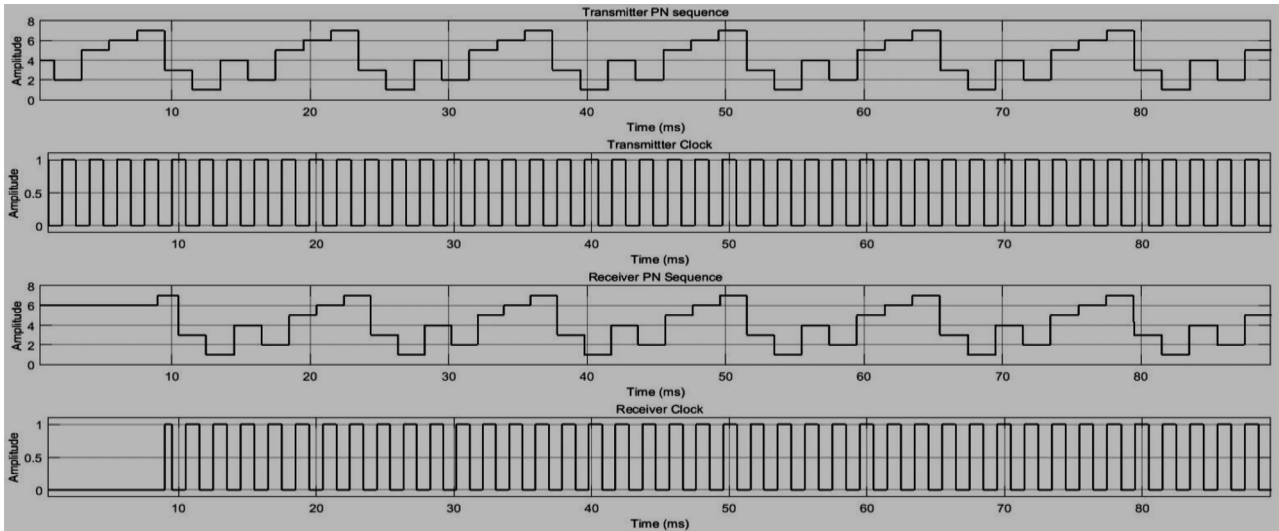


Figure 18. Receiver PN sequence lagging transmitter, alignment improvement highlighted by reference lines

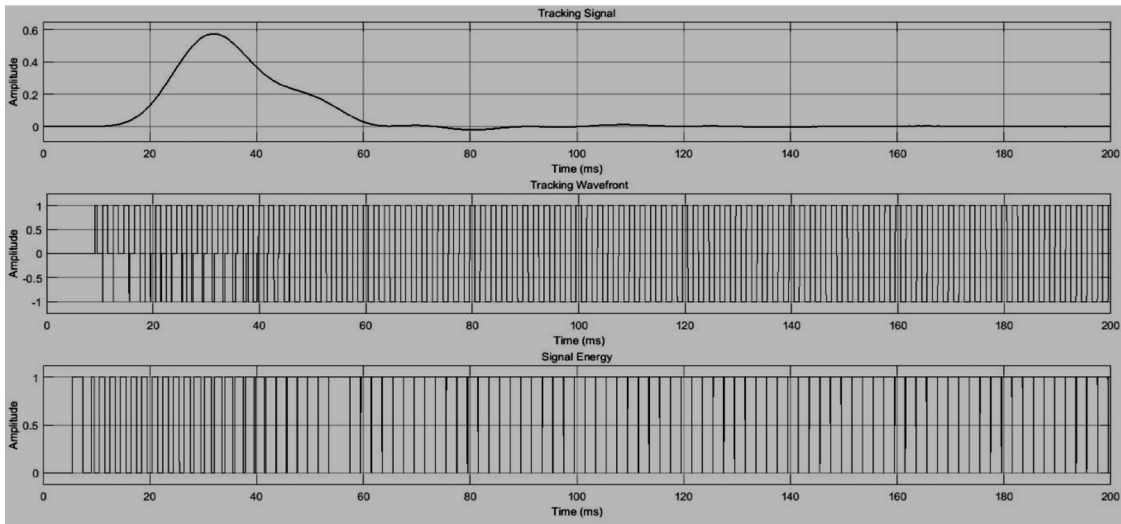


Figure 19. Tracking signals with receiver hopping pattern lagging transmitter hopping pattern

channel set to a signal to noise ratio of 10. The received binary output is only valid while the acquisition subsystem output is at 1. The period preceding this is utilized by the serial search subsystem to acquire the signal. A graph of the bit error rate (BER) against time (Fig. 14) shows that the system acquires the signal initially by waiting at the pre-set frequency and then initiates the process of hopping by enabling the clock that drives the PN generator. This is shown in Fig. 15.

The acquisition subsystem demonstrates that the receiver is not required to wait at a predetermined seed with the transmitter and start hopping simultaneously to transmit data.

This solves the problem of uncertainty of timing inherent in spread spectrum systems as the receiver hopping timing is

recovered from the transmitter. The acquisition time is directly related to the relative timing difference between the seed at the receiver and the current PN code the transmitter is broadcasting on.

3.3. Tracking subsystem

The acquisition system brings the transmitter and receiver PN code sequences into course alignment. The tracking subsystem initiates the process of achieving fine alignment of the PN sequences. This is shown in Fig. 16.

In Fig. 16, the PN sequence for the receiver is ahead of the sequence for the transmitter, hence the receiver hops to the next frequency carrier earlier than the transmitter. The



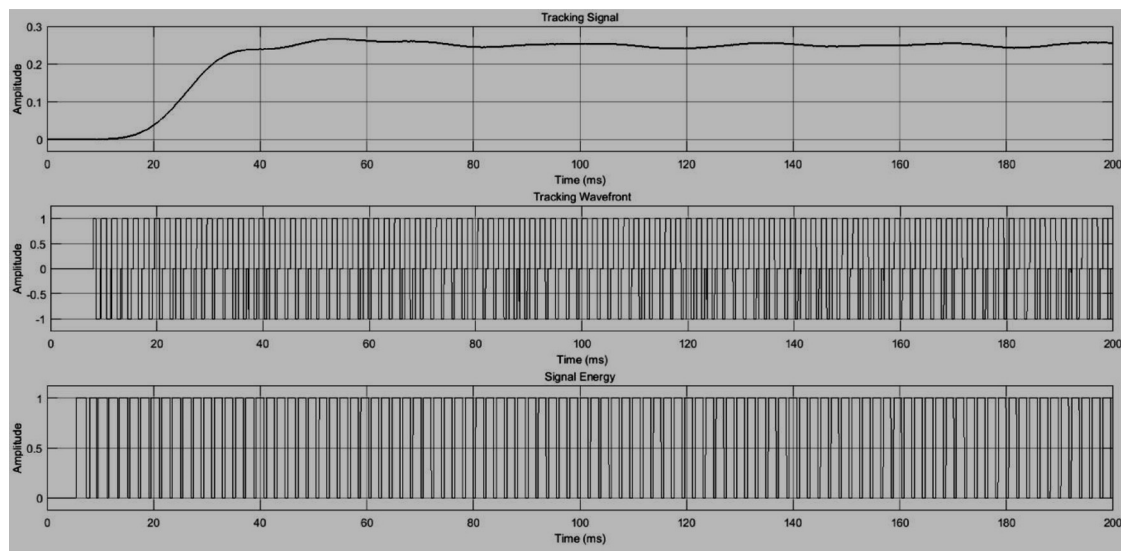


Figure 20. Tracking control voltage with transmitter +10Hz ahead of receiver

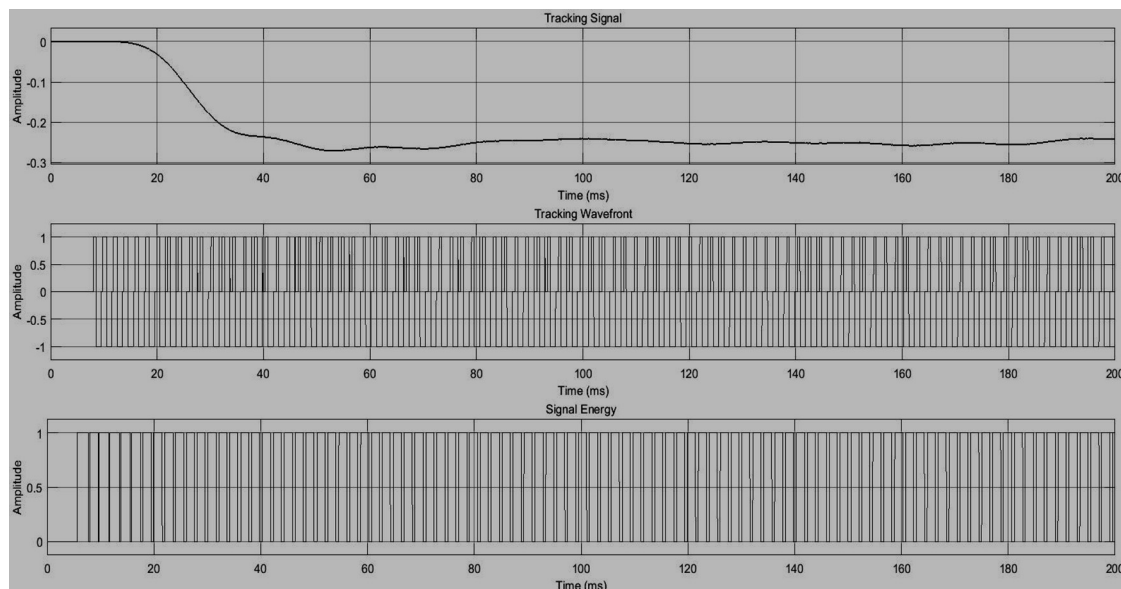


Figure 21. Tracking control voltage with transmitter 10Hz behind receiver

transmitter and receiver clocks are also seen to be out of alignment. As the system runs, the timing offset is reduced.

From the theoretical analysis, if the transmitter PN sequence lags behind the receiver PN sequence then a negative control voltage is expected at the VCC to slow down the receiver clock and allow the transmitter clock to catch up. As the code clock is brought into alignment, the control voltage of the VCC will tend towards 0V. This process is shown in Fig. 17.

From Fig. 18, the receiver hopping pattern is delayed behind the transmitter hopping pattern. The theoretical expectation is that the VCC will speed up its transitions to allow the receiver clock to catch up with

the transmitter clock. As soon as alignment is achieved, the VCC control voltage tends to 0V. This process is shown in Fig. 19.

The wave front of the tracking signal shows gradual improvement as the PN sequences are brought into fine alignment and the amount of energy the detector circuit obtains improves as well. The signal energy is seen to improve with the timing offset being eliminated from the signal.

The tracking signal will only tend to zero if both the transmitter and receiver clocks are running at the same quiescent frequency. The tracking subsystem also allows the receiver clock to be adjusted in frequency to compensate for frequency mismatch between the transmitter and receiver. If

the transmitter frequency is higher than the receiver, the tracking signal will settle at a positive value, while, if the transmitter frequency is lower than the receiver, tracking signal will settle at a negative value.

The tracking speed is controlled by the VCC sensitivity and the bandwidth of the Lowpass filter that produces the mean signal. The higher the VCC sensitivity, the greater the correction the tracking signal can apply and hence the faster the response of the tracking system.

Figures 20 and 21 show the behavior of the tracking system with a frequency offset of 10Hz between the transmitter and receiver code clocks.

The VCC oscillator that controls the timing of the VCC clock for the PN code generator has a sensitivity of 40Hz/V. The expected value of tracking signal that would lead to a frequency correction of $\pm 10\text{Hz}$ is $\pm 0.25\text{V}$. These values are shown in Figs 20 and 21.

4. CONCLUSION AND DISCUSSION

The objectives of the paper were achieved. FHSS systems were studied and the importance of code tracking was demonstrated. The importance of an acquisition system was also demonstrated. The system allows the receiver to adjust its clock frequency to match up the locally generated PN sequence with the received PN sequence. The tracking system prevented errors by ensuring the two PN sequences do

not go out of synchronization with each other, which would result in a loss of signal. The tracking system allowed for demodulation process to be more reliable by allowing a larger amount of signal energy to be received by the demodulator.

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